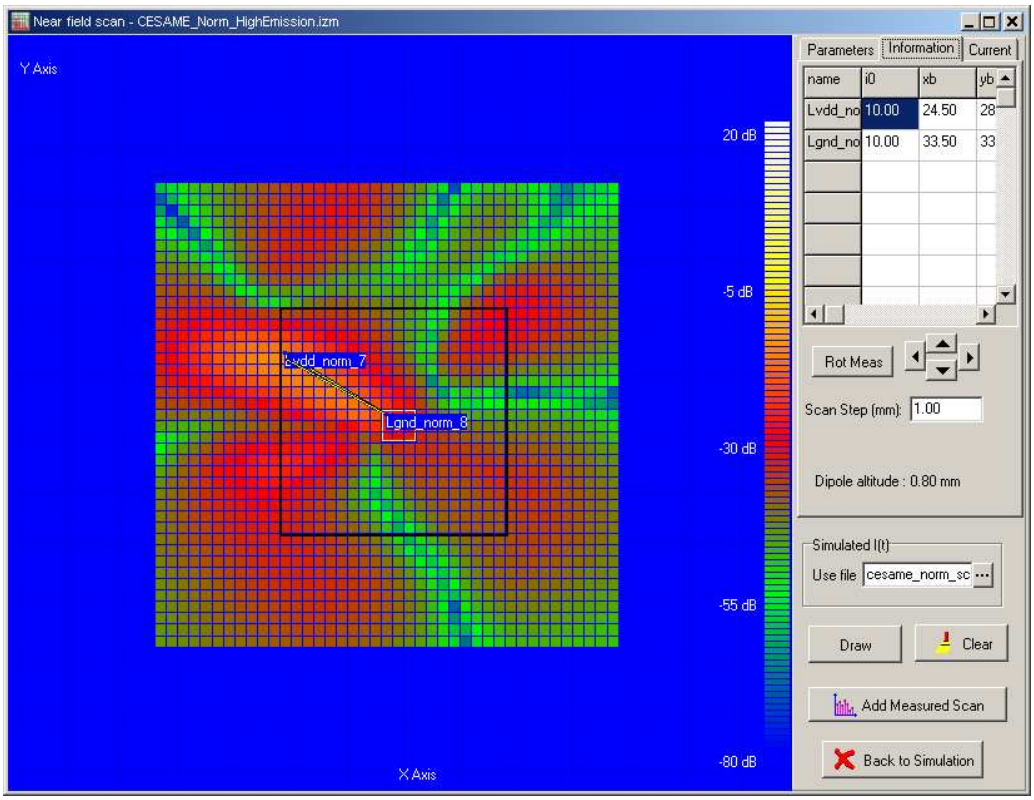
# IC-Emc
# User's Manual

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www.ic-emc.org

**March 2005**





ISBN **2-87649-048-X**
Published by INSA TOULOUSE, France, 2005

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## Abstract

This report describes the tool IC-EMC which aims at simulating parasitic emission based on ICEM models, and compare results with measurements. The tool uses the freeware WinSpice [1] derived from SPICE Berkeley for analog simulation. The ICEM model is illustrated and several examples of comparison between measurements and simulations are proposed, within the range 1MHz-1GHz.
The part on immunity simulation and comparison with measurements is also presented as well as the screen dedicated to near field scanning simulation based on ICEM.

# Table of Contents

# 1 Parasitic Emission of Integrated Circuits

Parasitic emission caused by the switching activity of integrated circuits (ICs) has increased in importance with the tremendous progress in Complementary Metal-Oxide Semiconductor (CMOS) technology. According to the International Technology Roadmap for Semiconductors (ITRS) [2], the 70nm CMOS process will be made available for production in 2005, featuring a standard operating frequency near 10GHz for processing units, and the capability to integrate within a 3x3cm silicon die several hundred thousands of gates, representing nearly one billion transistors (Table 1). When switching, each gate generates a small current pulse which flows mainly on the supply lines. The addition of these elementary current pluses provokes enormous current flows within the chip, close to 100A in the latest generation of high performance micro-processors.

Due to these transient currents, the ICs may generate conducted and radiated parasitic emission. The increase in operating frequencies, circuit complexity and number of I/Os is depicted in figure 1-1, according to the EDA roadmap [3]. It can be seen that the peak emission level also tends to increase, and may provoke severe interference inside and near the IC. Most measurement methods are limited to 1GHz. The GTEM measurement method, applicable to radiated emission up to 18GHz, is under standardization.

| **Year** | **2002** | **2005** | **2010** |
|---|---|---|---|
| CMOS Technology | 0.12 µm | 70nm | 35 nm |
| Internal Supply Voltage | 1.2 V | 0.7 V | 0.4 V |
| Max Area (mm²) | 22x22 | 25x25 | 30x30 |
| Interconnect Layers | 7 | 9 | 12 |
| Typ CPU Frequency (GHz) | 2 | 10 | 25 |
| Max number of Pads | 1800 | 2500 | 5000 |
| ***EMC*** | | | |
| Conducted Emission (dBµV) | 80 | 90 | 100 |
| Existing meas. methods | TEM, 1ohm | GTEM | unknown |
| Frequency range of interest: DC to | 3 GHz | 10 GHz | 30 GHz |
| I/O Modeling | IBIS v3 | IBIS v4 | unknown |
| Core Modeling | ICEM | ICEM xHF | unknown |

*Figure 1-2: The increase in EMI with the CMOS technology scale down*

There is a growing demand for low emission integrated circuits, especially in the automotive market. Several noise reduction techniques have already been proposed in technical papers and implemented successfully in industrial micro-controllers. Applying low emission design rules is usually efficient, but several questions rise:

- ⇒ is there an optimum value and placement for the on-chip decoupling capacitance?
- ⇒ Is the floor planning optimum regarding low parasitic emission?
- ⇒ To which extend would the block placement inside the IC affect the EMI?
- ⇒ Would new technological options such as bulk isolation reduce the emission?

Answering to such questions require accurate EMI models, adequate simulation tools and a reliable EMI prediction methodology.

This report described the use of a simple circuit model based on the ICEM standard [4], to obtain an accurate prediction of internal block switching up to 1GHz, in order to forecast conducted and radiated emission.

The report also describes near-field scanning simulation and comparison with measurements. The part dedicated to immunity simulation based on ICEM is also presented.

# 2 Flow for comparing measurements with simulations

## 2.1 General Flow

The simulation steps for comparing measured and simulated electromagnetic emission is described in figure 2-1. The IC supplier (top left) makes available an IBIS model and the ICEM model of its component (called IC_One). The ibis file IC_one.IBS contains I/O and package information. The file IC_one.CIR contains a sub-circuit description including internal current consumption information and die decoupling. In parallel, a test board is designed to perform conducted mode and radiated mode measurements according to international standard methods described in [5].

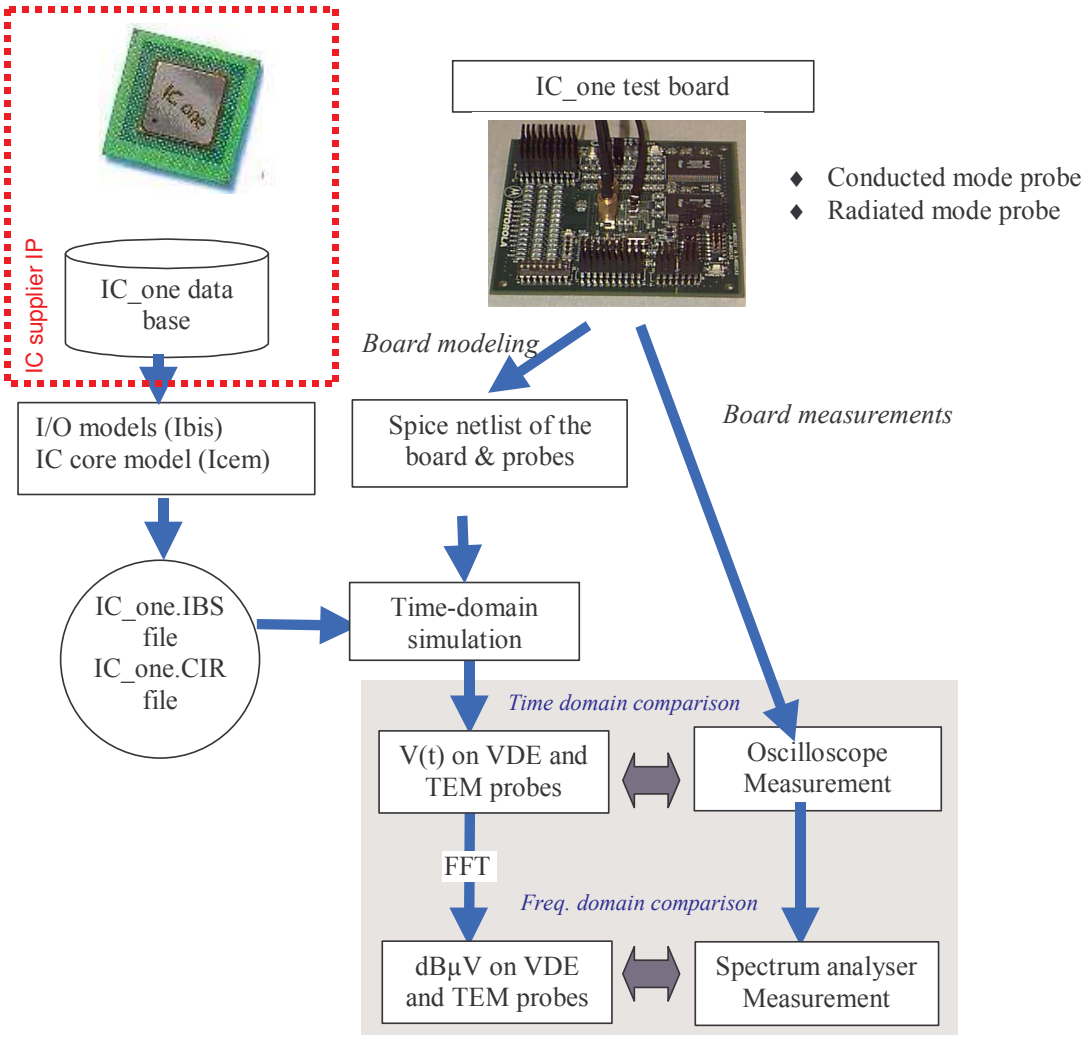



*Figure 2-2: Exploitation of ICEM and IBIS models to compare simulation and measurements*

## 2.2 The ICEM model basis


The objective of the ICEM model (Integrated Circuit Electrical Model) for Components is to propose electrical modeling for integrated circuit internal activities. This model will be used to evaluate electromagnetic behavior and performances of electronic equipment. The ICEM proposal issued from the UTE task force has been submitted to the IEC standardization committee under reference IEC 62014-3.

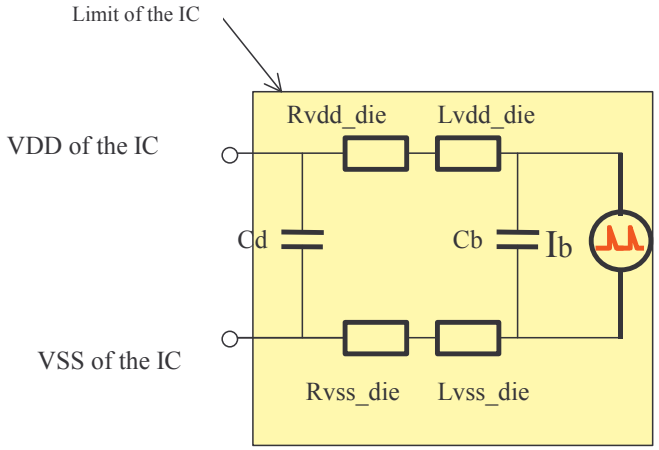



*Figure 2-3*: The ICEM model and logo

A short description of ICEM is provided in this paragraph. The complete description may be found in the cookbook of ICEM [6]. The core model structure includes the decoupling capacitance *Cd*, the serial resistance *Rvdd_die, RVss_die* and serial inductance *Lvdd_die, Lvss_die* on the supply rails. It also separates the capacitance into two contribution: *Cd*, between VDD and VSS, and *Cb*, close from the current generator *Ib* (Figure 2-4).

| | | |
|---|---|---|
| `Ib` | Current source.<br>Unit: Ampere<br>Description: piece-wise-linear | Main source of parasitic emission considered in the model is the current source Ib. The current shape may consist either of the time-domain description of the current versus time or as an equivalent triangular waveform. Typical values for Ib are several mA, up to 1A for the amplitude, 0.5 to 5ns for duration, and 500ps to 50ns for the period. |
| `Cd` | Decoupling capacitance.<br>Unit: Farad<br>Description: discrete C | On-chip decoupling capacitance between VDD and VSS. Cd is a physical coupling between the internal supply rails VDD (positive supply) and the ground rail VSS (0V supply). The origin of the capacitance Cd is rail to rail or junction capacitance. Typical value ranges from 100pF (very small Ics) up to 20nF (0.18µm System-on-chip). |
| `Lvdd_die, Lvss_die` | Serial internal inductance.<br>Unit: Henry<br>Description: discrete L | The serial inductance Lvdd_die, Lvss_die, in serial with the local block capacitance Cb creates a high frequency resonance effect. Typical value ranges from 0.1nH (very short connection to supply) up to 10nH (long connection). |

| | | |
|---|---|---|
| Rvdd_die, Rvss_die | Serial internal resistance.<br>Unit: Ohm<br>Description: discrete R | The serial resistance of the supply network models the path that connects the block supply to the main supply ring. Typical value for Rvdd, Rvss are 0.5 to 50 ohm. |
| Cb | Block decoupling capacitance.<br>Unit: Farad<br>Description: discrete C | The local block decoupling Cb is the local supply-to-ground capacitance placed in serial with the local current generator Id. It accounts for the equivalent decoupling capacitance of the block. Separating the block capacitance from the on-chip capacitance Cd creates a second LC network (Lvdd, Cb, Lvss) at the origin of a secondary resonance. |

# 3 ICEM in the schematic editor

## 3.1 Download the Schematic Editor

The schematic editor may be downloaded from www.ic-emc.org [7]

⇒ Click the item "Download", and chose “IC-EMC" in the software section.
⇒ Save the ZIP file on your hard disk, preferably in a new directory, for example called "Ic-emc" in "Program Files".
⇒ Unzip the contents of the file
⇒ Double click the executable file ICEM.EXE

## 3.2 Dowload WinSpice

WinSPICE may be downloaded from www.winspice.com.

## 3.3 Getting started with the schematic editor

The main screen of the schematic editor is shown in figure 3-1. The editor contains a palette of symbols (Window "Symbol Library" situated on the right of the screen) and some basic editing icons to build the schematic diagram of the circuit. The R,L,C components may be found in the "Advanced" index of the symbol library.

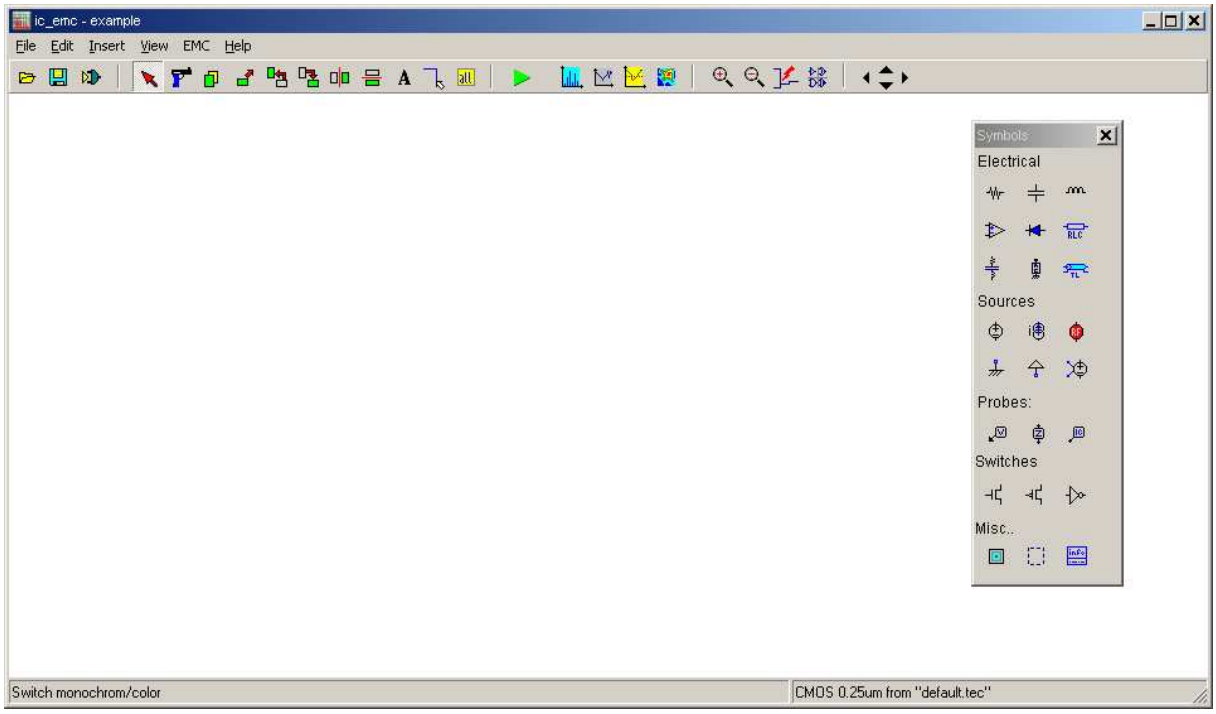



*Figure 3-2: the default screen of the schematic editor*

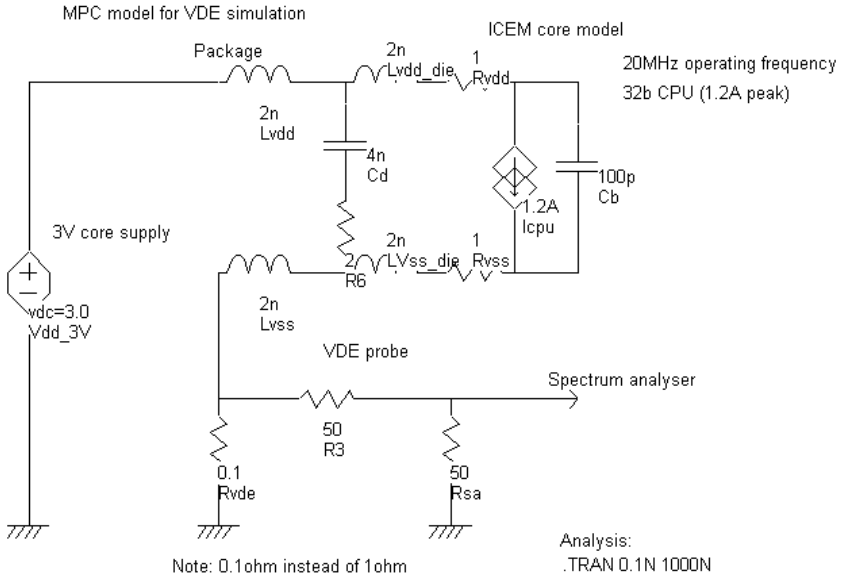



*Figure 3-3: The ICEM model of a 32bit micro-controller (mpc_vde.SCH)*

Load the file "mpc_vde.sch" which corresponds to figure 3-4. A 32bit micro-controller is described using basic RLC elements of the ICEM model, the IBIS elements for the package, and the VDE probe.

| Parameter | Description | *Remarks* |
|---|---|---|
| Ib | Current source.<br>Unit: Ampere<br>Description: piece-wise-linear | *The Ib current is described as a periodic triangle (1.2A max)* |
| Cd | Decoupling capacitance.<br>Unit: Farad<br>Description: discrete C | *Cd is 5nF, which is quite high due to on-chip added capacitance* |
| Lvdd_die,<br>Lvss_die | Serial internal inductance.<br>Unit: Henry<br>Description: discrete L | *The serial inductance is tuned to 2nH, which provokes a resonance effect with Cb around 300MHz.* |
| Rvdd_die,<br>Rvss_die | Serial internal resistance.<br>Unit: Ohm<br>Description: discrete R | *Around 2 ohm serial resistance due to long metal tracks on-chip* |
| Cb | Block decoupling capacitance.<br>Unit: Farad<br>Description: discrete C | *Local block capacitance, around 100pF.* |

Elements concerning the package are Lvdd and Lvss, accounting for the serial equivalent inductance from the die of the IC to the physical supply source, and the VDE probe. Notice that the serial resistance is 0.1ohm instead of 1ohm, as the current flowing inside the IC is very big. Putting a 1ohm serial resistance would dissipate nearly 1Watt and induce a voltage drop near 1V.

## 3.4 Create the SPICE file

Invoke the command *File → Generate Spice file* or click <Ctrl>+<G>. The following screen appears.

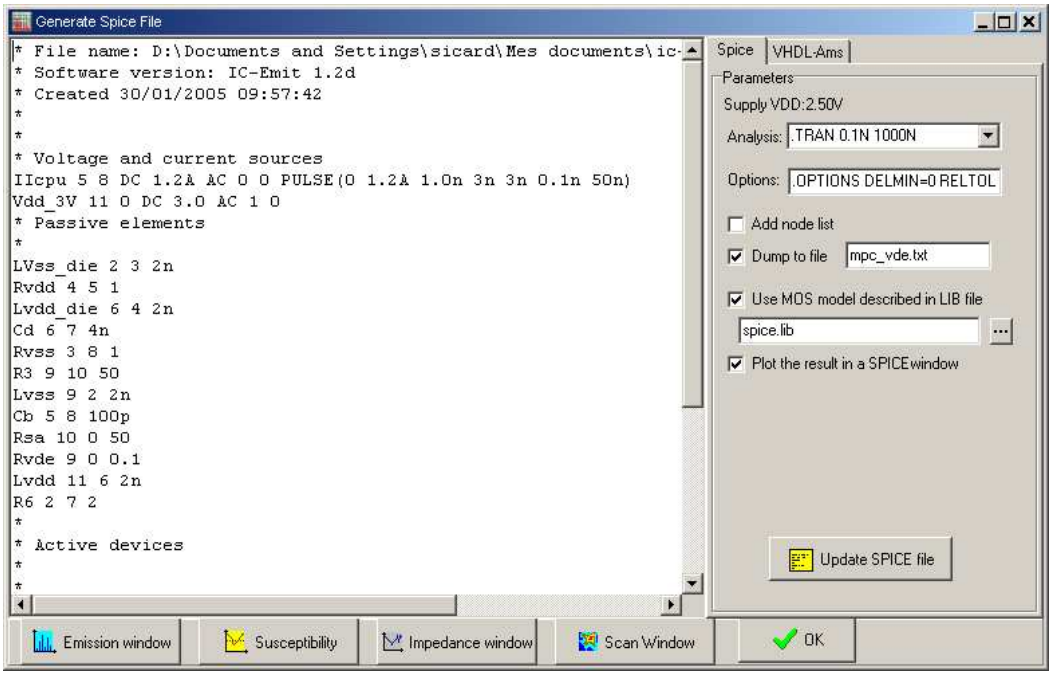



*Figure 3-5: the SPICE file generated from the schematic diagram (mpc_vde.SCH)*

The description of ICEM parameters in SPICE is based on SPICE reference manual [8].

| | |
|---|---|
| RESISTOR<br>RXXXXXXX N1 N2 VALUE<br>Example: Rvss 3 7 2ohm | N1 and N2 are the two element nodes. VALUE is the resistance (in ohms) and should be positive. |
| CAPACITOR<br>CXXXXXXX N+ N- VALUE<br><IC=INCOND><br>Example: Cb 6 2 1n | N+ and N- are the positive and negative element nodes, respectively. VALUE is the capacitance in Farads. |
| INDUCTOR<br>LYYYYYYY N+ N- VALUE<br>Example: Lvss 8 2 2n | N+ and N- are the positive and negative element nodes, respectively. VALUE is the inductance in Henry. |
| CURRENT SOURCE<br>IYYYYYYY N+ N- <<DC><br>DC/TRAN VALUE><br>Example: IB 23 21 DC 0.01 | N+ and N- are the positive and negative nodes, respectively. A current source of positive value forces current to flow out of the N+ node, through the source, and into the N- node.<br>DC/TRAN is the dc and transient analysis value of the source. If the source value is zero both for dc and transient analyses, this value may be omitted. If the source value is time-invariant (e.g., a power supply), then the value may optionally be preceded by the letters DC. |
| Supply voltage<br>VYYYYYYY N+ N- <<DC><br>DC/TRAN VALUE><br>Example: VDD 1 0 DC 2.0V | N+ and N- are the positive and negative nodes, respectively. A voltage source of positive value is set between N+ node, and N- node. |

## 3.5 Current Source Description

The current source is assigned a time-dependent value for transient analysis. There are five independent source functions: pulse, exponential, sinusoidal, piece-wise linear, and single-frequency FM. In the schematic editor, the PULSE description has been implemented, as shown in figure 3-6.

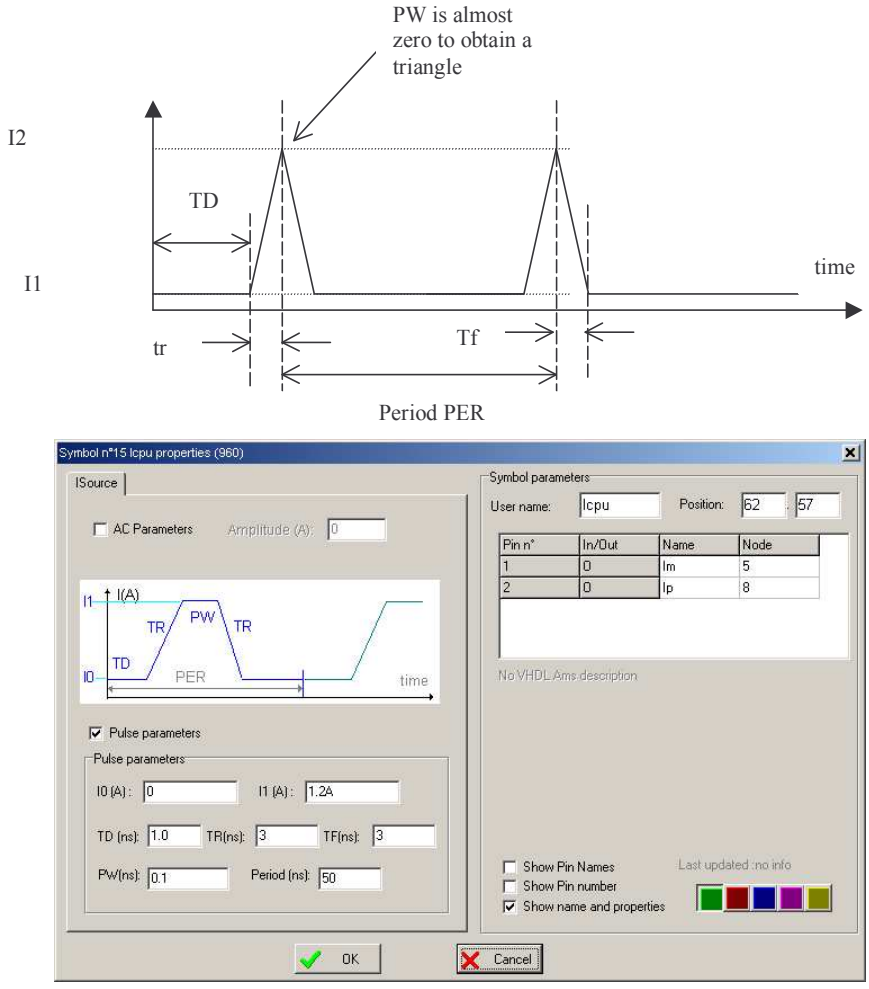



*Figure 3-7: Current Pulse parameters in the schematic editor*

The PULSE description restricts the *Ib* shape to a periodic pulse, which has a triangular shape if the pulse width parameter is set to zero.

```
PULSE(I0 I1 TD TR TF PW PER)
Example: IIcpu 5 7 PULSE(0 1.2A 1.0n 3n 32n 0.1n 50n)
```

| | | |
|---|---|---|
| I0 | initial value | Amps |
| I1 | pulsed value | Amps |
| TD | rise time | TSTEP seconds |
| TF | fall time | TSTEP seconds |
| PW | pulse width | TSTOP seconds |
| PER | period | TSTOP seconds |

## 3.6 Voltage Source Description

The voltage source is assigned a constant value to modelize the supply source. In figure 3-8, the voltage source is constant, with a DC value of 3V.

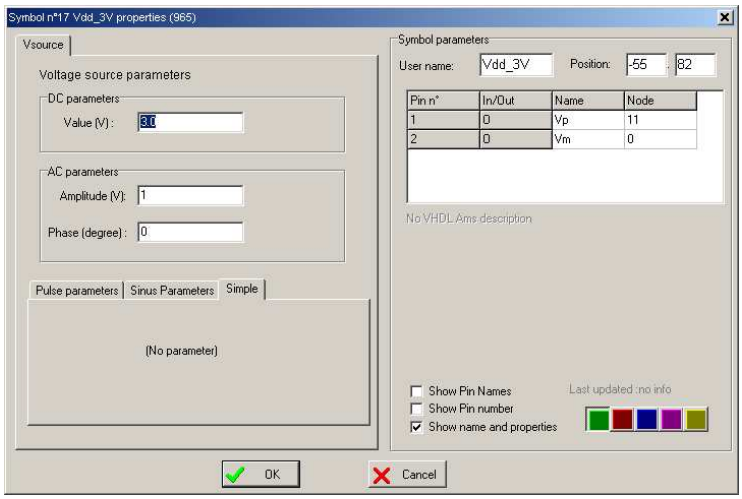



*Figure 3-9 :* Constant voltage source

## 3.7 Analysis Description

In the editing window, a text is added which sets up the desired analysis. The text must start by '.TRAN' (Transient analysis), '.AC' (Small signal frequency analysis), or '.DC' (static characteristics). In figure 3-10, the time-domain analysis is set to 1000NS, with a simulation step of 0.1NS.

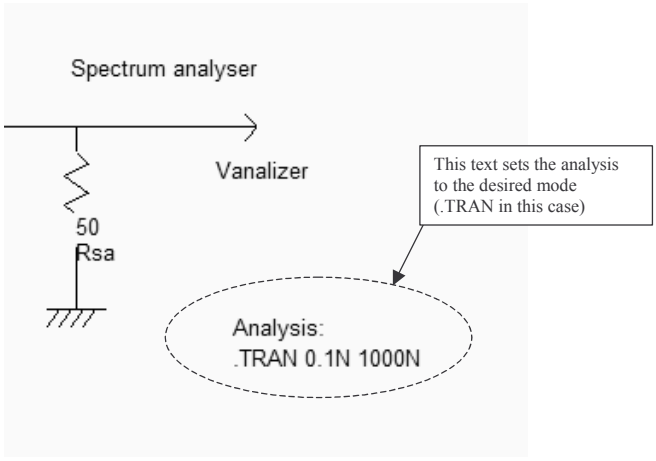



*Figure 3-11 :* Defining the SPICE simulation parameters

## 3.8 Run SPICE Simulation

Start the WinSpice program, and click "File" → "Open". Select the desired .CIR file. In our example (Figure 3-12), the file generated by DSCH is "mpc_vde.CIR".

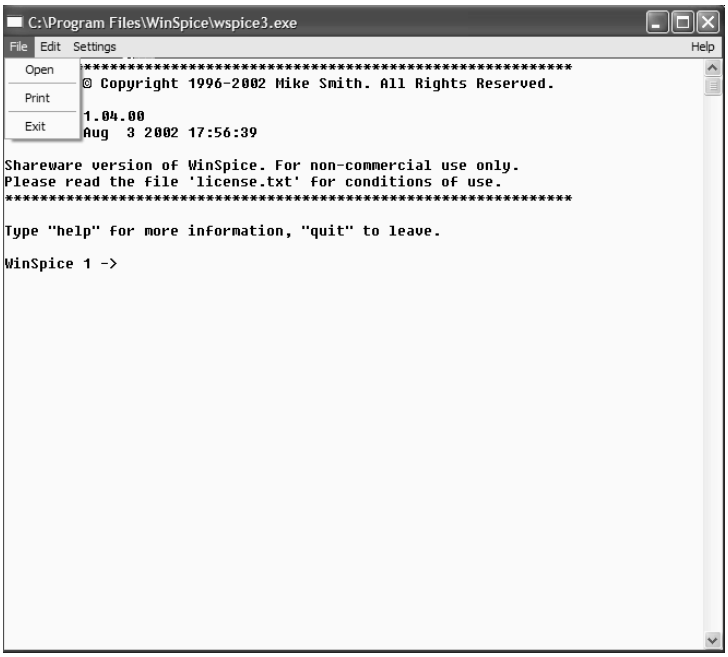



*Figure 3-13: The WinSpice initial screen*

The simulation is performed in time domain, and the following screen appears. The .TRAN analysis is conducted during 1000NS. The result is stored in a file called `mpc_vde.txt`. The plot of the transient simulation appears in a new window reported in figure 3-14.

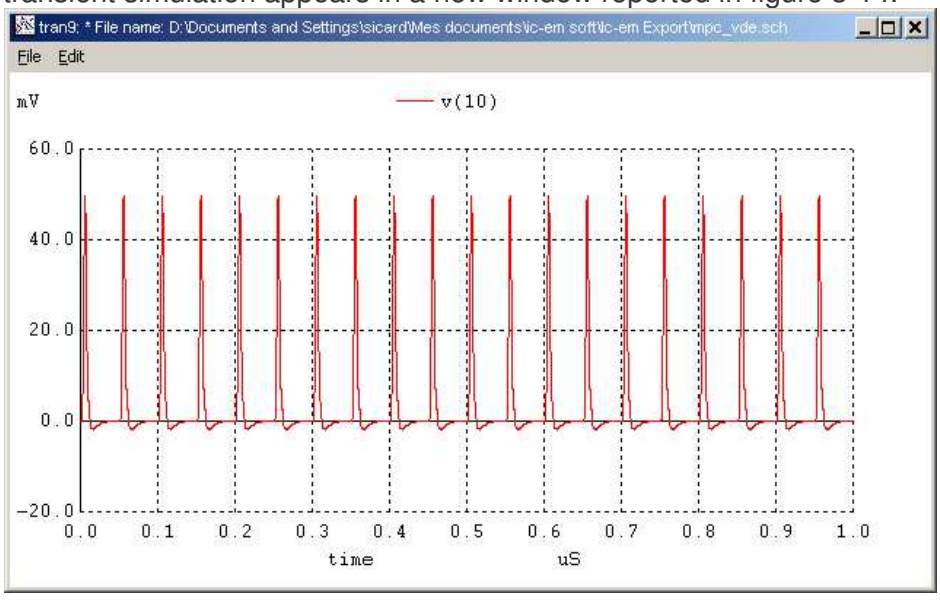



*Figure 3-15: the transient simulation performed by WinSpice*

## 3.9 Post Processing

The voltage waveform computed by the analog simulator must be translated by Fast Fourier Transform (FFT) into frequency domain energy. The X axis should cover the range 1-1000MHz in logarithmic scale. The representation of the energy in Y axis should be made in dBµV, equal to 20*log(V*1e6). The table of correspondence is shown in figure 3-16. In other words, 1µV should correspond to 0dBµV, 1mV to 60dBµV and 1V to 120dBµV.

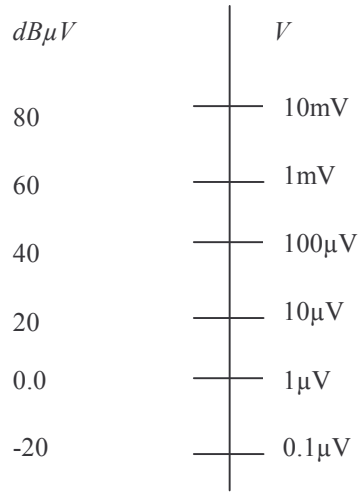



*Figure 3-17 : Correspondence between V and dBµV*

In the SPICE generator menu, click "EMC Window", or click "View" → "EMC Window with FFT". A specific screen with Log/Log units configured to display energy vs frequency is proposed, as shown in figure 3-18. In the item "Use file", click the button [...] and select the file "mpc_vde.txt". The spectrum appears as shown in the figure. The FFT points are adapted to fit the information included in the simulation.

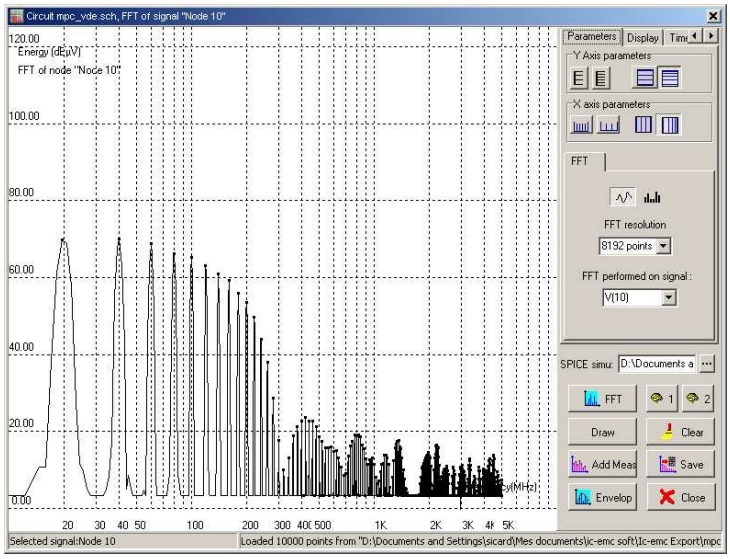



*Figure 3-19: Simulation of the conducted emission of the MPC*

## 3.10 Comparison with Measurements

In the EMC window, click "Add Measurements" to display the measurements superimposed to the simulations, for comparison purpose. An example of comparison is proposed in figure 3-20, and concerns the MPC, a 32-bit micro-controller for automotive applications.

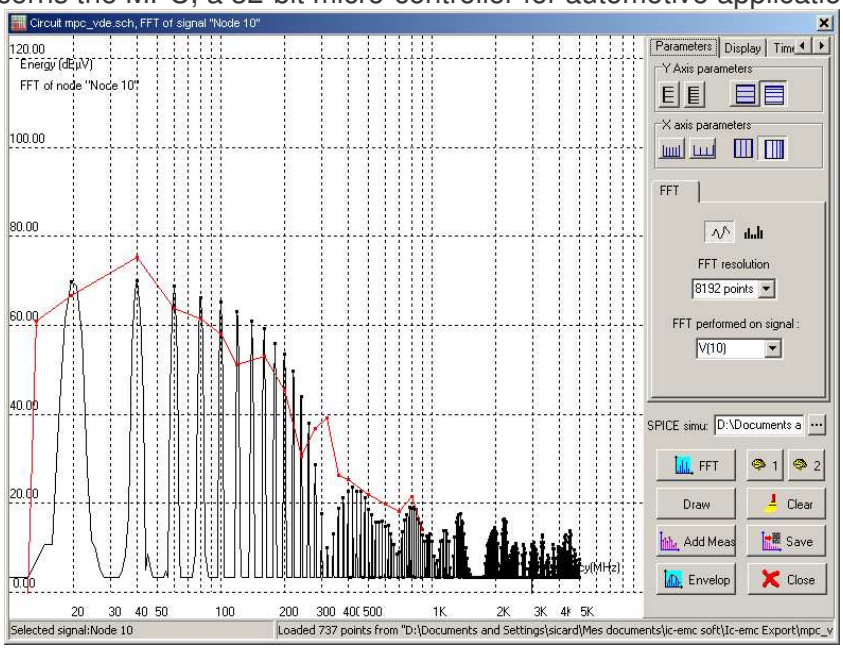



*Figure 3-21 : Comparison between measured and conducted emission of the MPC processor*

## 3.11 Discussion

The simulation is well fitted with measurements, as seen in figure 3-22. The main spectrum energy is concentrated in the range 10-300MHz, with low levels of energy above 300MHz. The ICEM model remarkably predicts the 20-100MHz harmonics. However, some discrepancies are observed from 100 to 300MHz (Up to 10dB difference).

The ICEM parameters may be fitted to improve the accuracy of the prediction in that range. Possible approaches may consist in:

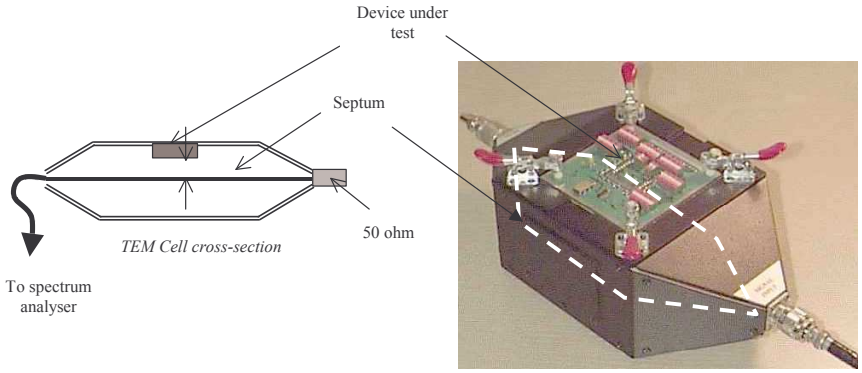
- ⇒ Altering the PULSE current parameters: the rise slope TR or fall slop TF may be modified, as well as the peak current value (I2).
- ⇒ Replacing the PULSE current by a PWL current. The current generator is simply a triangular peak, while the real current is far more complex. The PWL current includes more information which may change the harmonic contents, and thus improve the matching between measurement and simulation.
- ⇒ Alter the values of the block capacitor Cb and the serial inductor Lvdd_die, LVss_die. This modifies the second order resonance effect.

# 4 ICEM in Radiated Mode

This section describes the use of ICEM for predicting the measured radiated emission in TEM cell.

## 4.1 The TEM Cell Model

The TEM cell picture and model are proposed in figure 4-1. The core of the cell consists in a 50 ohm adapted metal plate in a grounded chamber. The metal plate is called septum. The septum model consists of two inductors and a capacitor. For symmetry, the total septum inductor is split into two inductors Ltem1 and Ltem2, 10nH each . The capacitance of the septum vs. the ground is around 8pF.



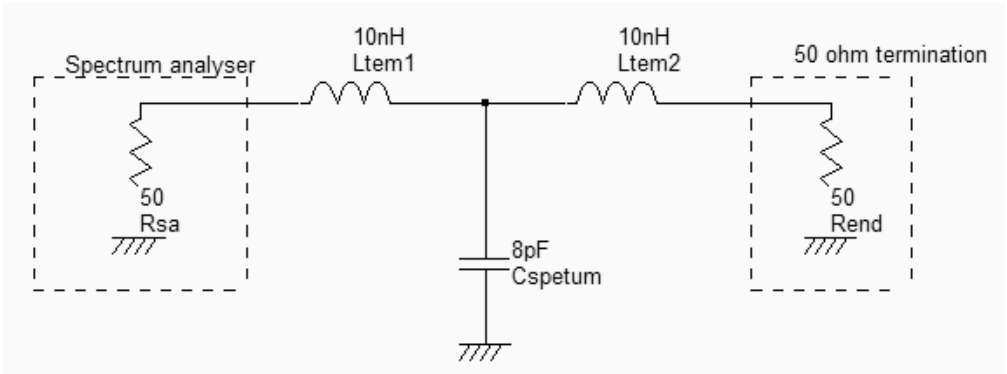




*Figure 4-2 : The TEM cell model (temModel.SCH)*

## 4.2 Coupling between the IC and the TEM Cell

In the ICEM model, two main coupling phenomena have been identified:

⇒ Capacitance coupling between the die and the septum

⇒ Inductance coupling between the package and the septum

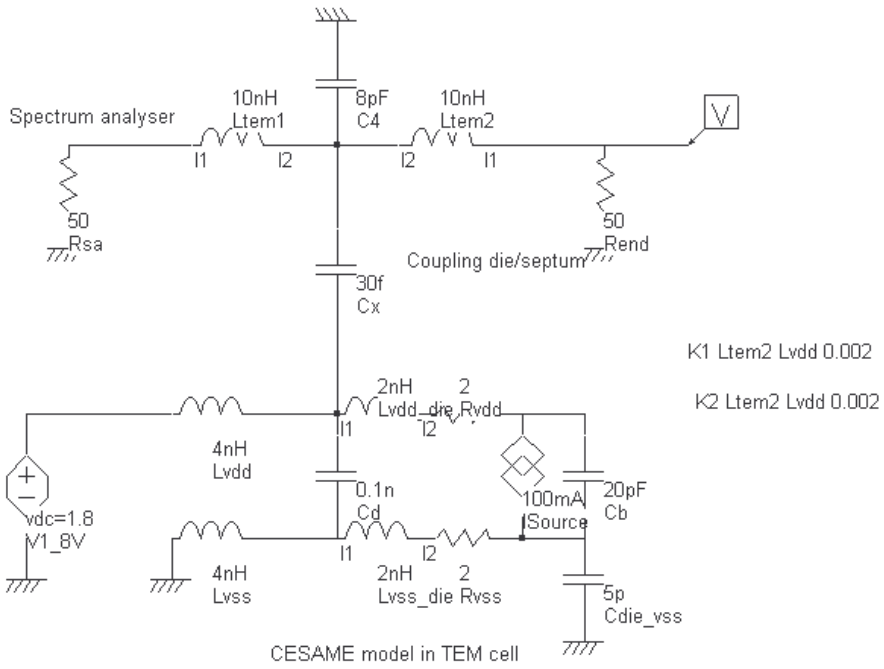



*Figure 4-3 : A model of the CESAME test chip in the TEM cell (cesame_tem_norm.sch)*

The capacitance coupling between the IC and the septum is represented by *Cx*, with a value of 30fF (Figure 4-4). The inductance coupling between the VDD supply inductance *Lvdd* and the septum inductance *Ltem1*, *Ltem2* is represented by a Coupling factor K. The coupling element K is added as a label, with a syntax as follows. The coupling value here is 0.002, equivalent to 0.2%. This low value is due to VDD and VSS routed close, that reduce the coupling K by almost 20dB. Normal value for K is 1% between a package lead and the septum.

```
Kxxx Lyyy Lzzz coef
Example: K1 Ltem1 Lvdd 0.002
```

To modify the coupling value, double click inside the label, and change the number (0.002 in the figure 4-5) to the desired value.

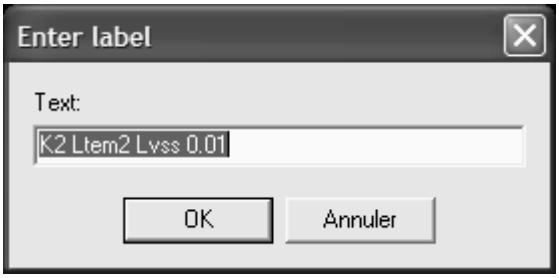



*Figure 4-6: Modifying the coupling factor between two inductors*

## 4.3 Comparison between measurements and simulations

A comparison between measurements (In red) and simulation (In black) is proposed in figure 4-7. It can be seen that a reasonable agreement is found up to 1GHz. The simulation is significantly higher than measurements above 700MHz.

Notice that the I/O switching that occurs in real-case measurements at a rate of 10MHz provokes harmonics starting from 10MHz. In the model, this switching has been ignored.

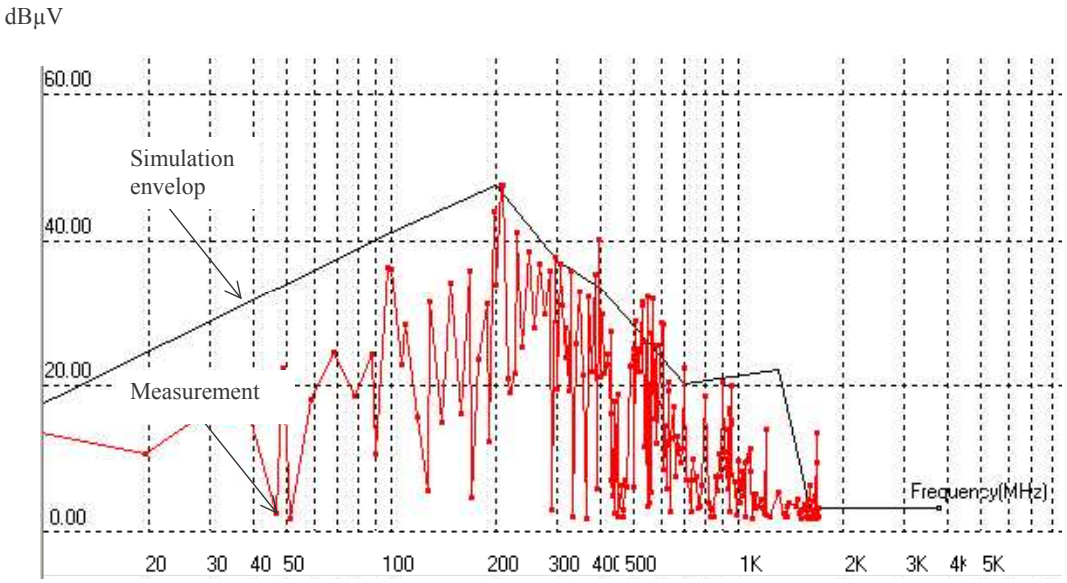



*Figure 4-8 : Comparing simulation and measurements of the CESAME test chip in the TEM cell (cesame_tem_norm.sch)*

# 5 Comparing measured and simulated Impedance

## 5.1 Impedance simulation

An example of impedance simulation using IC-EMC is shown in figure 5-1. The supply impedance of an integrated circuit (C51 microcontroller) is represented by the on-chip decoupling C1, the access package inductance LVdd, LVss, as well as parasitic serial resistance Rvdd and Rvss. The software uses a specific probe called "Z probe" that can be found in the probe menu, close to the voltage probe. The Z probe is inserted between the two electrical nodes where the impedance needs to be measured.

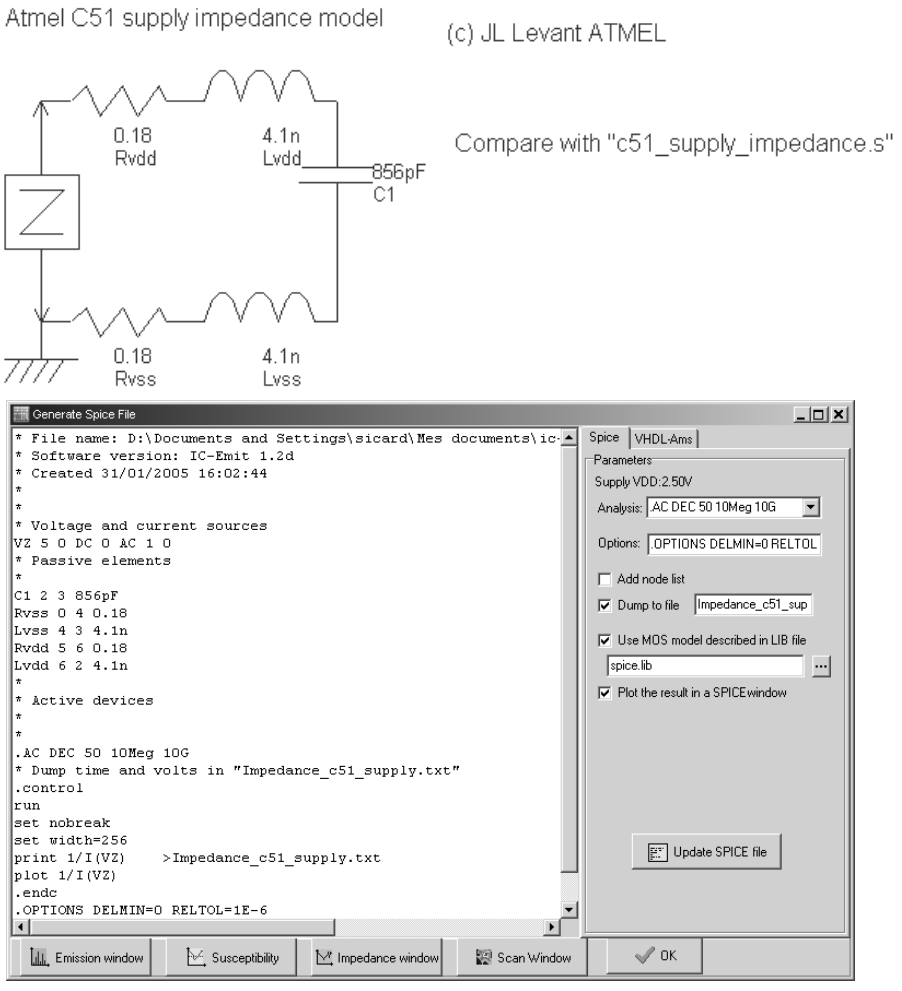



*Figure 5-2: The impedance simulation in IC-EMC uses a specific Z probe*

We start WinSpice, select File → Open *impedance_c51_supply.CIR.* The AC simulation is started, and the output file is *impedance_c51_supply.TXT.* It contains the module of the impedance.

The simulator will use the defined AC Source combined with a probing of the current. The result is plotted on a specific window by a click in “Impedance Window” from the Spice interface (Figure 5-3). The ratio between the voltage and current has been automatically computed from 10MHz to 10GHz (See the Spice netlist).

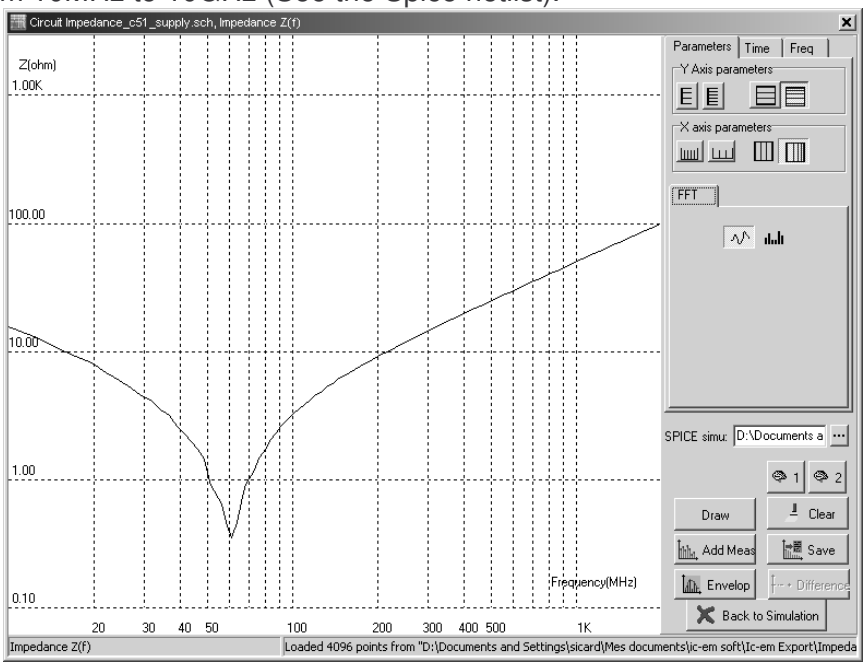



*Figure 5-4: The impedance simulation result using WinSpice*

## 5.2 Comparing measurements and simulation

We compare here measurements from [S] parameters with impedance simulations. The conversion procedure in IC-Emc uses the following equations:

$$S11 = R + jX$$

$$Zin(real) = Z_0\left(\frac{1-R^2-X^2}{(1-R)^2+X^2}\right)$$

$$Zin(imag) = Z_0\left(j\frac{2X}{(1-R)^2+X^2}\right)$$

$$|Zin| = \sqrt{Zin(real)^2 + Zin(imag)^2}$$

An example of [S] parameter data file is shown below. Notice the three columns: frequency (Hz), real part of S11, imaginary part of S11. The appendix for this type of measurement file is '.S'.

```
PCB board Jan 04
Mesures S11(f)
Freq (Hz) Reel Im
1000000 0.882568359     -0.468902588
```

```
1004326.68      0.881835938     -0.470703125
1008672.081     0.880554199     -0.472717285
1013036.282     0.87979126      -0.474334717
1017419.366     0.878875732     -0.476348877
1021821.414     0.877929688     -0.477966309
```

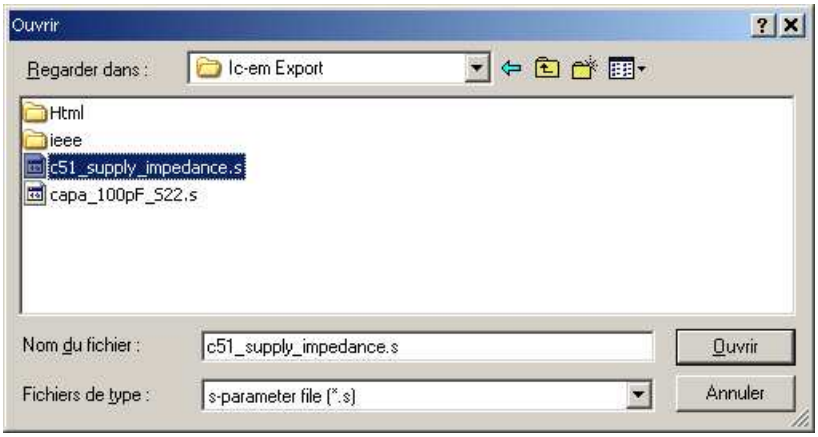



*Figure 5-5: Loading a [S] parameter impedance measurement file*

We select the button "Add measurements", select the data format as shown in figure 5-6.

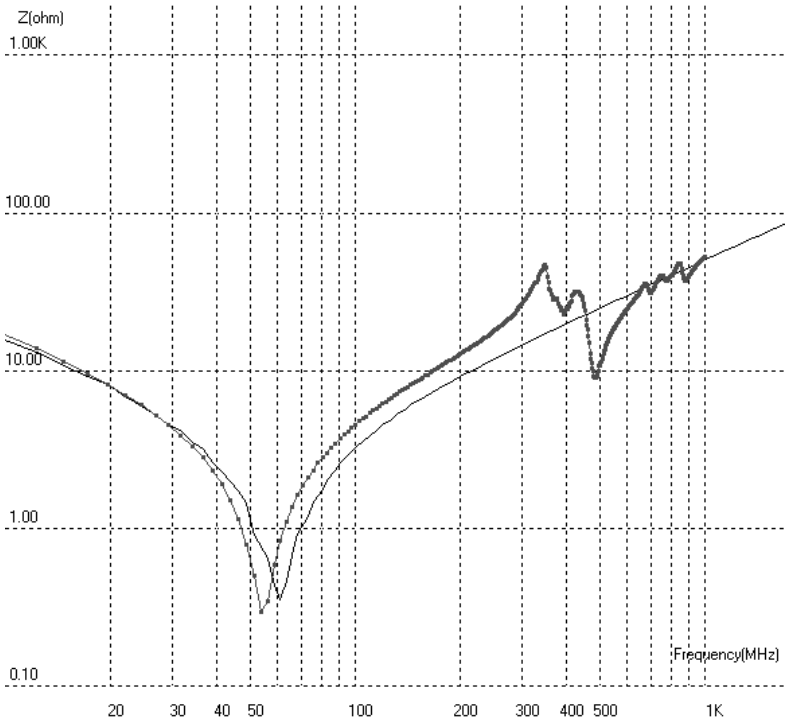



*Figure 5-7: Measured and simulated impedance*

The correlation is quite good, as shown in figure 5-8. Notice the 10MHz shift between the impedance calculated from [S] measurements and the simulation.

## 5.3 R,L,C in High frequencies

In his PhD thesis, Luca Giaccoto [9] has measured the impedance of a discrete capacitor (100pF) up to 10GHz. A simple model valid up to 1GHz is shown in figure 5-9. The measurement file is provided in [s] parameters (A5_100pF_S22.s). The IC-Emc pre-processor converts [s] tabulated data into impedance as detailed in a previous section.

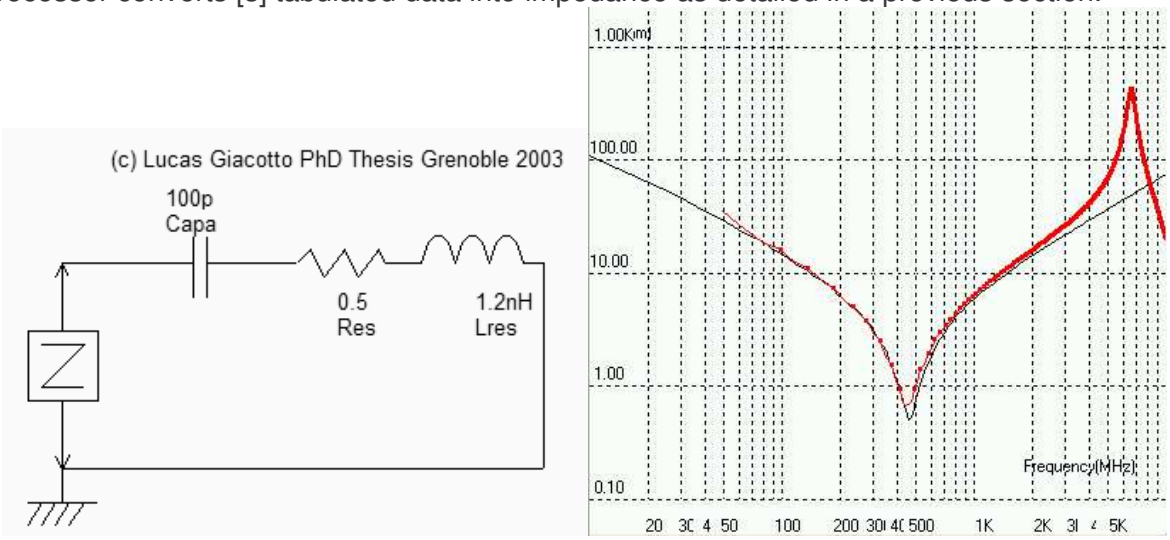



*Figure 5-10: High frequency models for a discrete capacitor (capa_100pf_hf.SCH)*

The impedance of discrete capacitor may be approximated by the circuit shown in figure 5-11, up to 10GHz. The same [s] measurement file is used (A5_100pF_S22.s).

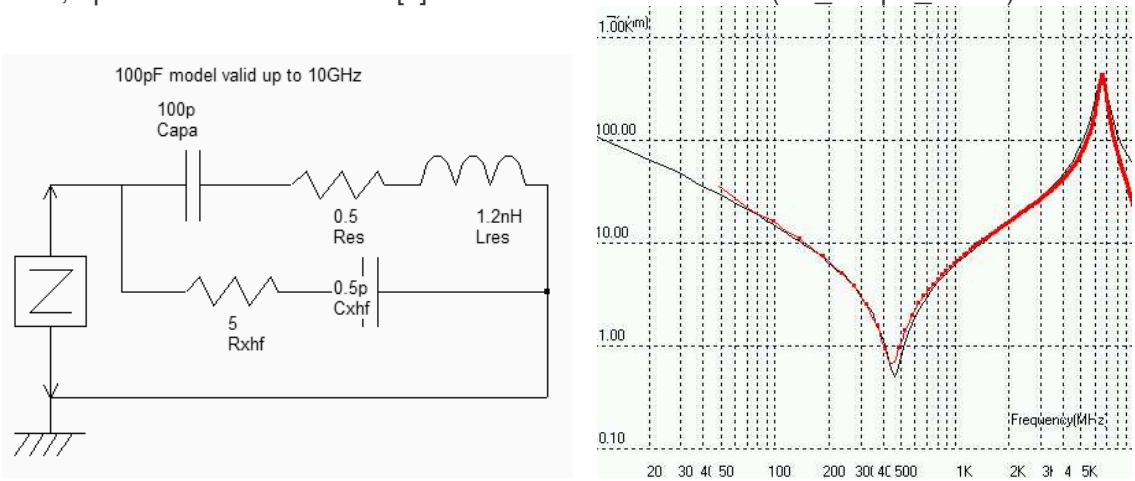



*Figure 5-12 : Extremely high frequency model for a discrete capacitor (capa_100pf_xhf.SCH)*

# 6 IBIS Support

## 6.1 Introduction

The software IC-EMC is able to extract RLC information from IBIS files in a simple way. Using the command **File → Load Ibis File**, the following screen appears (Figure 6-1).

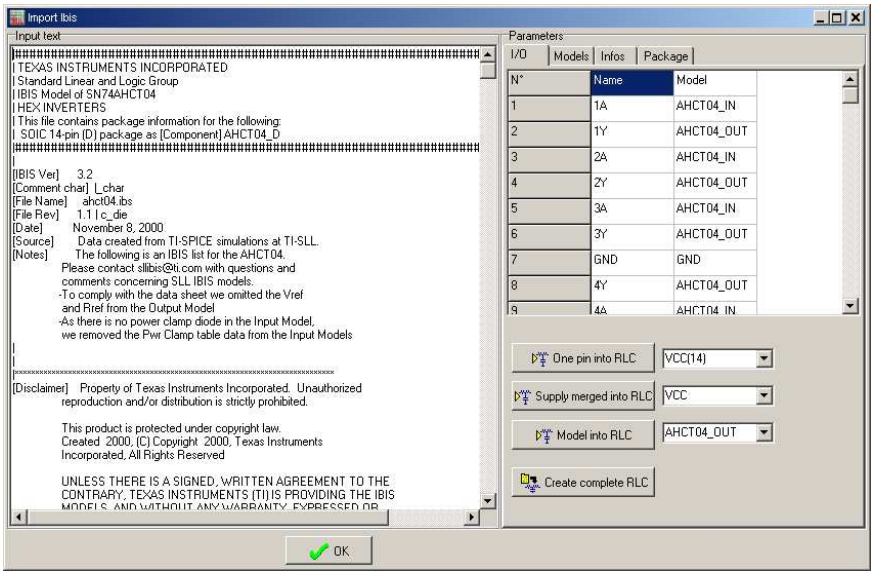



*Figure 6-2: Loading an IBIS file in IC-EMC (File ahct04.Ibs from Texas Instruments)*

## 6.2 Convert an input into RLC diagram

Click the desired input pin in the I/O list, then click the button "One pin into RLC". The input pad is converted into a RLC circuit with on-chip capacitance and clamp, as shown in figure 6-3. It consists, from left to right, in a button with the input name (Here '2A'), the R,L,C parameters for the package (Here L1,C1,R1), the component input capacitance (Ccomp2), and the clamp diode (Clamp).

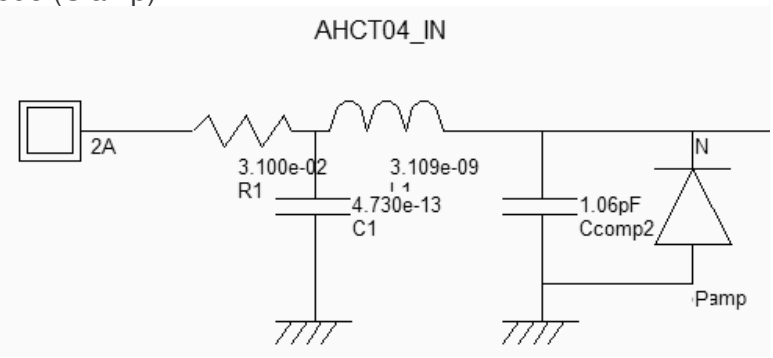



*Figure 6-4 : Model of the '2A' input pad (File ahct04.Ibs from Texas Instruments)*

## 6.3 Diode Modeling

The clamp appearing in figure 6-5 must be tuned to fit the *i/v* characteristics given in the IBIS file. The i/v characteristics appear in figure 6-6, by a simple click in the "Models" item from the IBIS window, and by selecting the gnd_clamp (GC) or power_clamp (PC) model in the selector, if it exists. If the button is not selected, this means that no data has been provided in the IBIS file for the corresponding *i/v* curve.

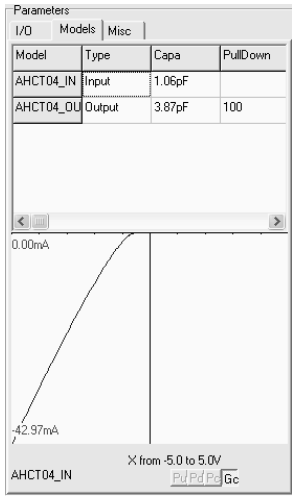
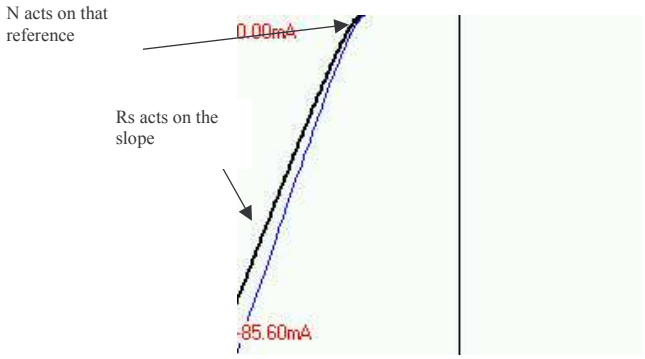



*Figure 6-7: Clamp characteristics (File ahct04.Ibs from Texas Instruments)*

The user must build a SPICE model for the clamp diode that fits the given characteristics. The diode model includes the following basic parameters (All other parameters may be ignored for simplicity).




| Parameter | Description | Typical |
|---|---|---|
| Is | Saturation current | $10^{-14}$ A |
| N | Emission coefficient | 1 |
| Rs | Ohmic resistance | 10ohm |
| vj | Junction potential | 0.7V |
| fc | Forward bias junction fit parameter | 0.5 |
| Bv | Reverse breakdown voltage | 10V |
| ibv | Current at reverse breakdown voltage | $10^{-3}$ A |

*Figure 6-8: Basic diode parameters*

## 6.4 Comparison between IBIS and Winspice Diode characteristics

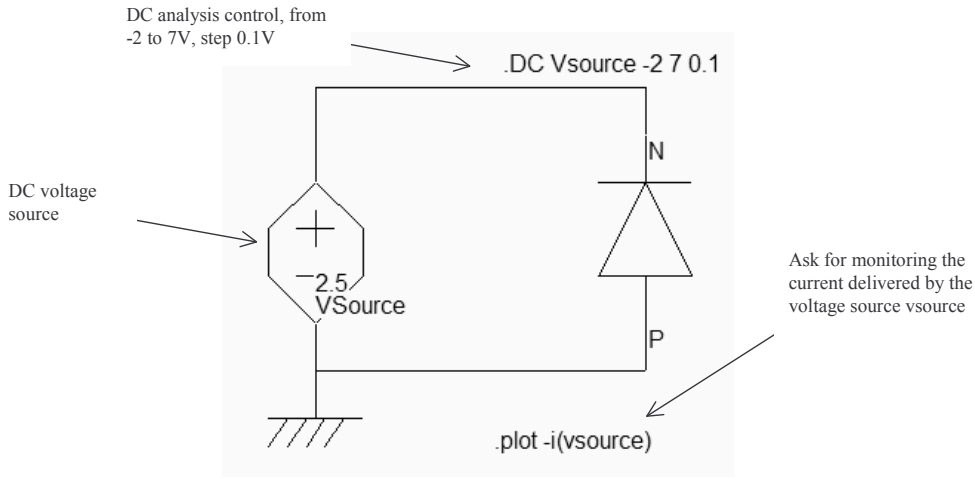



*Figure 6-9: Setup for DC simulation of the clamp diode (diode_dc.SCH)*

The WinSpice simulation of the i/v characteristics is performed by the following script. The corresponding schematic diagram is given in figure 6-10. Notice that the diode model uses most default parameters except for the serial resistance (10 ohm instead of 0) and the junction potential (0.8 instead of 0.7V).

| | |
|---|---|
| `*`<br>`VSource 2 0 DC 2.5 AC 1 0`<br>`*`<br>`D1 0 2 clamp`<br>`.model clamp D Rs=10 N=0.8`<br>`*`<br>`.DC Vsource -2 7 0.1`<br>`*#run`<br>`*#set nobreak`<br>`*#print -i(vsource) > diode_dc.txt`<br>`*#plot -i(vsource)`<br>`.OPTIONS DELMIN=0 RELTOL=1E-6`<br>`.END` | `Comment`<br>`Voltage source declaration`<br>`Comment`<br>`Diode between nodes 0 and 2, model 'clamp'`<br>`Diode model: only change Rs and N`<br>`Comment`<br>`DC analysis from -2 to 7V, step 0.1V`<br>`Start analysis`<br>`No break in simu`<br>`Dump I(v) result in file 'diode_dc.txt'`<br>`Also show the graphical result after simu`<br>`Some options`<br>`End process` |

The analysis gives the result shown in figure 6-11.

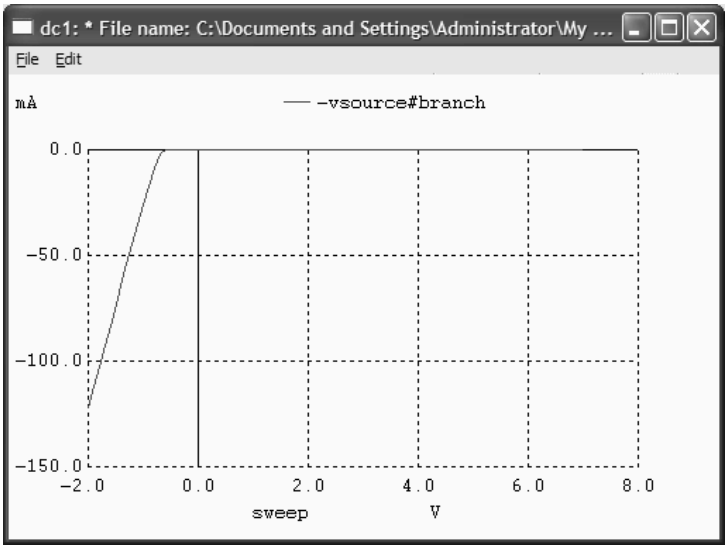



*Figure 6-12: WinSpice simulation of the clamp diode (diode_dc.SCH)*

The simulated data and the IBIS information may be compared by a click in the button "simu" situated on the lower right corner of the window. We choose the WinSpice data file 'diode_dc.txt' to enable the comparison between the IBIS and spice information. The comparison example is provided in figure 6-13.

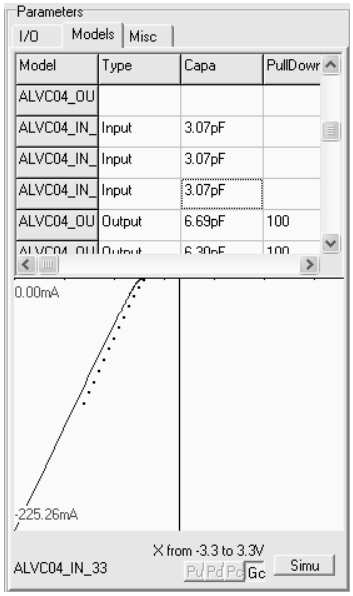



*Figure 6-14: Comparing IBIS data and simulation of the clamp diode (diode_dc.SCH)*

## 6.5 Converting an output

Now, choose the desired output pin in the list and click the button "One pin into RLC". The output pad is modelized by the RLC elements of the package and the on-chip capacitance as for the input pad. One n-channel MOS device and one p-channel MOS device are added to the schematic diagram to account for the buffer.

The schematic diagram of figure 6-15 shows an example of output buffer model. It consists, from left to right, in the n-channel and p-channel MOS devices, the R,L,C parameters for the package (Here L1,C1,R1), the pad capacitance (Ccomp2), and the arrow.

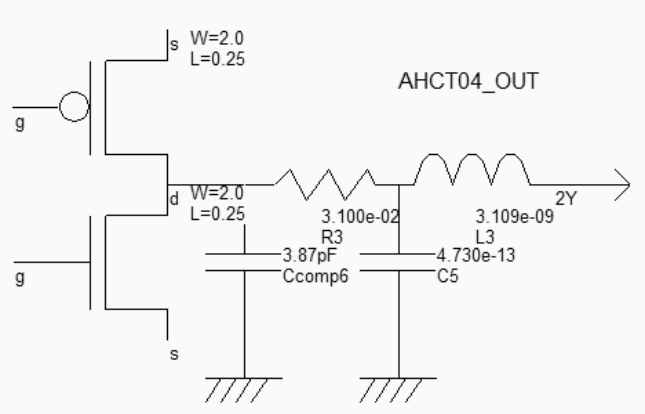



*Figure 6-16 : Model of an output pad (File ahct04.Ibs from Texas Instruments)*

The MOS devices appearing in figure 6-17 must be tuned to fit the *i/v* characteristics given in the IBIS file. The i/v characteristics appear in figure 6-18, by a simple click in the "Models" item from the IBIS window, and by selecting the pull_up (PU) or pull_down (PD) models in the selector, if it exists. If the button is not selected (Such as PC and GC in figure 6-19), this means that no data has been provided in the IBIS file for the corresponding *i/v* curve.

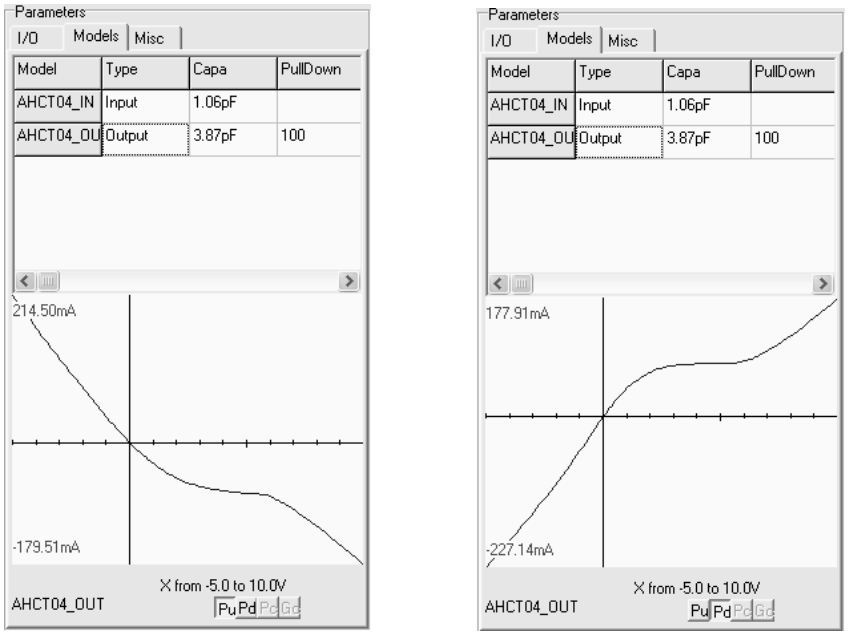



*Figure 6-20: i/v curves for the pull_up and pull_down devices (File ahct04.Ibs from Texas Instruments)*

## 6.6 Comparing IBIS and Winspice MOS characteristics

We use the basic MOS model 3 which provides a good compromise between simulation efficiency and accuracy. However, more advanced models such as BSIM4 [10] also supported by WinSpice may be used. The basic setup is shown in figure 6-21.

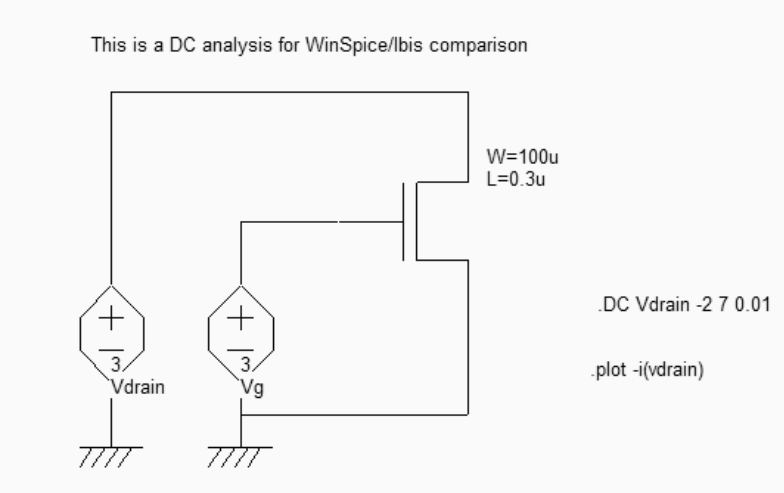



*Figure 6-22 : The simulation setup to produce the nMOS i/v characteristics (nmos_dc.SCH)*

The simulated data and the IBIS information may be compared by a click in the button "simu" situated on the lower right corner of the window. We choose the WinSpice data file 'nmos_dc.txt' to enable the comparison between the IBIS and spice information. The comparison example is provided in figure 6-23. The main fitting parameter is the MOS width W. It is not recommended to change the MOS model parameters, nor to decrease the channel.

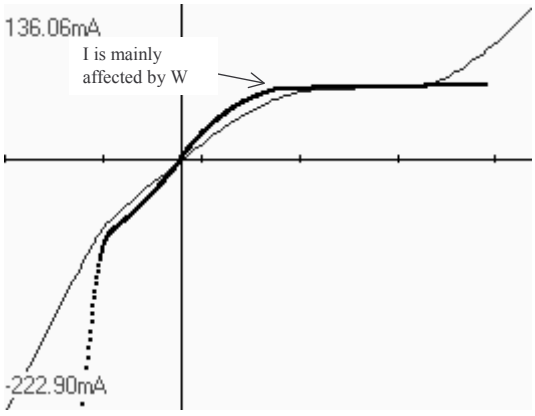



*Figure 6-24 : Comparing IBIS data and simulation of the nmos device (nmos_dc.SCH)*

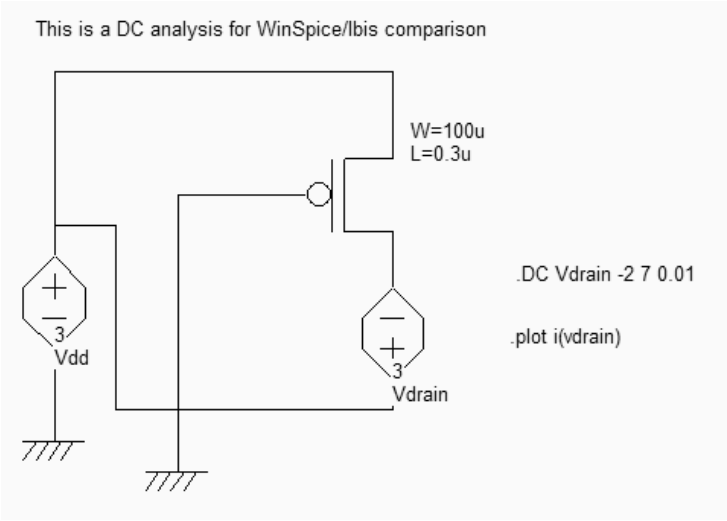



*Figure 6-25: Simulation setup for the pmos device (pmos_dc.SCH)*

We perform the same study for the pMOS. The simulation setup is a little tricky as shown in figure 6-26. The simulated data and the IBIS information may be compared by a click in the button "simu" situated on the lower right corner of the window (Figure 6-27).

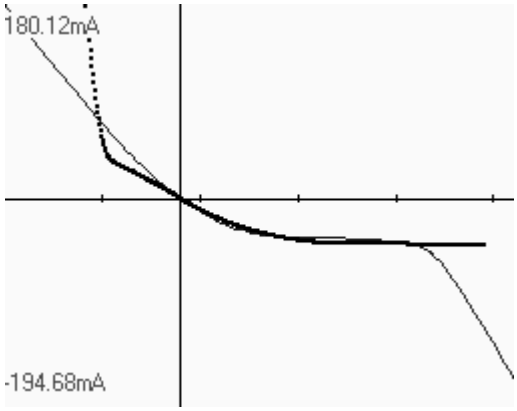



*Figure 6-28 : Comparing IBIS data and simulation of the pmos device (pmos_dc.SCH)*

## 6.7 Package Viewer

The aspect of the IC may be shown (figure 6-29), with details on the supply structure. The example below concerns a BGA from Infineon (TC1796).

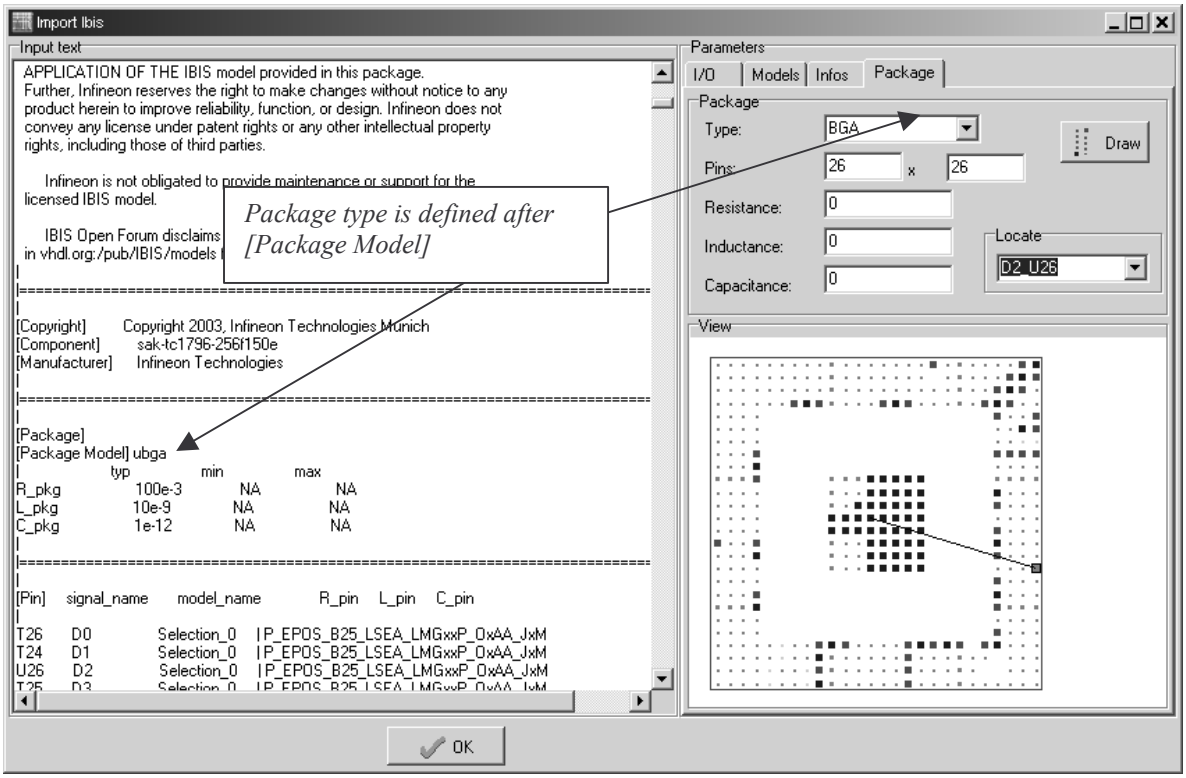



*Figure 6-30: Package viewer (infineon_tc1796.ibs)*

The package viewer uses [Package Model] keyword to configure the type of package. The following keywords (Figure 6-31) are handled by IC-Emc.

| Keyword | Type | IBIS example file |
|---|---|---|
| [Package Model] ubga | Micro BGA | infineon_tc1796.ibs |
| [Package Model] sop | SOP package | ahct04.ibs |
| [Package Model] qfp | Quad Flat Pack (QFP) | Cesame_v14.ibs |
| [Package Model] dil | Dual in line (DIL) | |

*Figure 6-32 : Examples of package declaration in the ibis file*

# 7 An Expert System to Generate ICEM models

This sections describes a specific tool that aims at generating automatically an ICEM model from high-level specifications of the integrated circuit technology, topology and gate complexity.

## 7.1 The ICEM Expert Interface

The screen of the ICEM model expert is reported in the figure below.

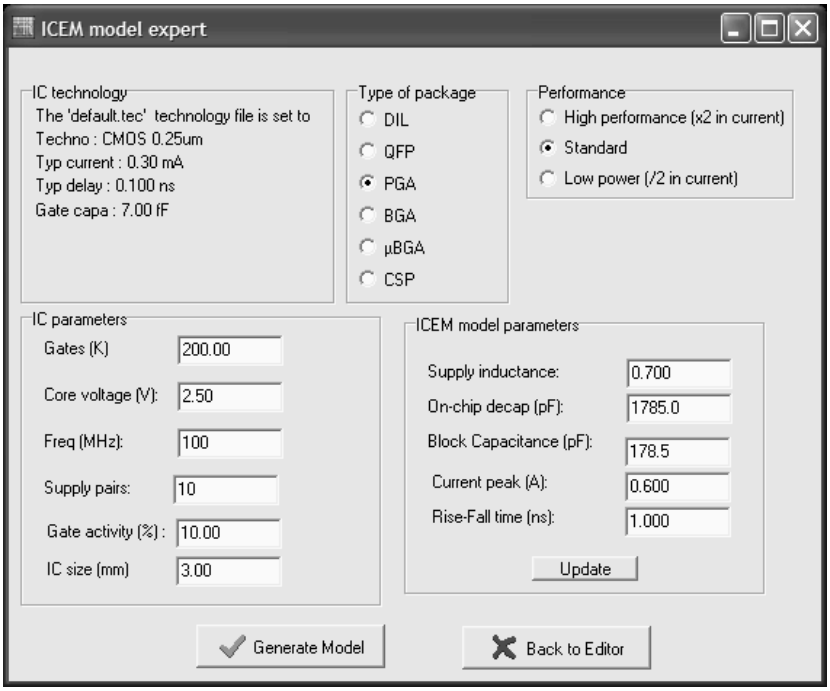



*Figure 7-1: The ICEM model generator and its user's interface*

On the left upper corner of the window, the default technological parameters are listed. These parameters are provided in the configuration file "default.tec", which is described in the appendix. The parameters worth of interest are:

- The typical switching current per gate (0.3mA in this technology)
- The typical duration of the gate switching (100 ps in the above example)
- The default gate decoupling capacitance (7fF)

The next menu, called "Type of package", selects the family of package, which has a direct impact on package inductance. The "performance" menu tunes the current peak (Ib) by increasing the peak current by 100% in "high speed" mode as compared to standard mode. In "low power" mode, the current is reduced by 50%.

In the lower left corner, several parameters that have a direct impact on the ICEM model are given:

- The number of gates (200Kgates in the example)
- The operating frequency (100MHz)
- The supply pairs (Number of VDD/VSS pins, 10 here)
- The % of switching activity in each active edge of the clock (10% proposed here)
- The IC size in mm (3x3mm in this example)

## 7.2 ICEM model example

A result example corresponding to the default expert system parameters is given in figure 7-2. The current generator is situated on the right side, with its local block capacitance. The serial access resistance *rdie_vdd* and inductance *ldie_vdd* and linked to the decoupling capacitance *Cdec*, which is connected to the supply inductance *lpack_vdd*.

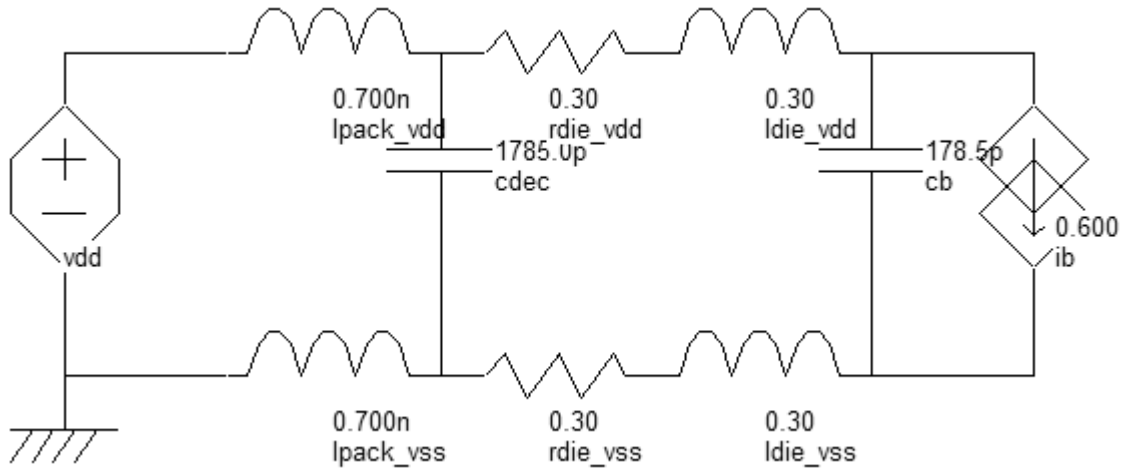



*Figure 7-3: An example of ICEM model generated automatically*

## 7.3 ICEM Parameter Computation

The computation of the ICEM elements is performed using the following approximations:

| | |
|---|---|
| Ldie_vdd = ic_Size*inductanceFactor;<br>Rdie_vdd = ic_Size*resistanceFactor; | The serial inductance and resistance are proportional to the size of the die. The factors are around 0.1, if the ic size in in mm. |
| imax=icPerfo*Gates*typ_current* Gate_Activity/spreadFactor; | The peak current of the source Ib is compute using several parameters: the spread factor is around 10; icPerfo is equal to 2 for high performance, 1 for standard and 0.5 for low power option. |
| tr := typ_Delay*SpreadFactor; | The rise and fall time of the current source is multiplied by the spread factor. |
| Lpack_vdd :=L_package/SupplyPairs; | The serial inductance is divided by the number of pairs. The inductance per pin depends on the package technology (15nH for DIL down to 1nH for CSP). |

| | |
|---|---|
| Cd := Gate_Capa*Gates+<br>icSupplyPairs*ioCapa+<br>icSize*icSize*SurfaceCapa; | The decoupling capacitance is the sum of the gate capa, the Io capa and the die surface capacitance. |
| Cb := Cd/10 | The local block capacitance Cb is 10 times lower than the total capacitance |

# 8 Signal Integrity with IC-Emc

## 8.1 Case study

We consider a test circuit (figure 8-1) with the following characteristics:

- Model of a 3.3V IC supply network (Vdd_IO, Lvdd_Io, Rdc_io, Cd_io, Lvss_io).
- A CMOS buffer (nMOS and pMOS) with a pad capacitor Ccomp
- 10mm package lead length
- 100mm PCB track
- 10pF termination

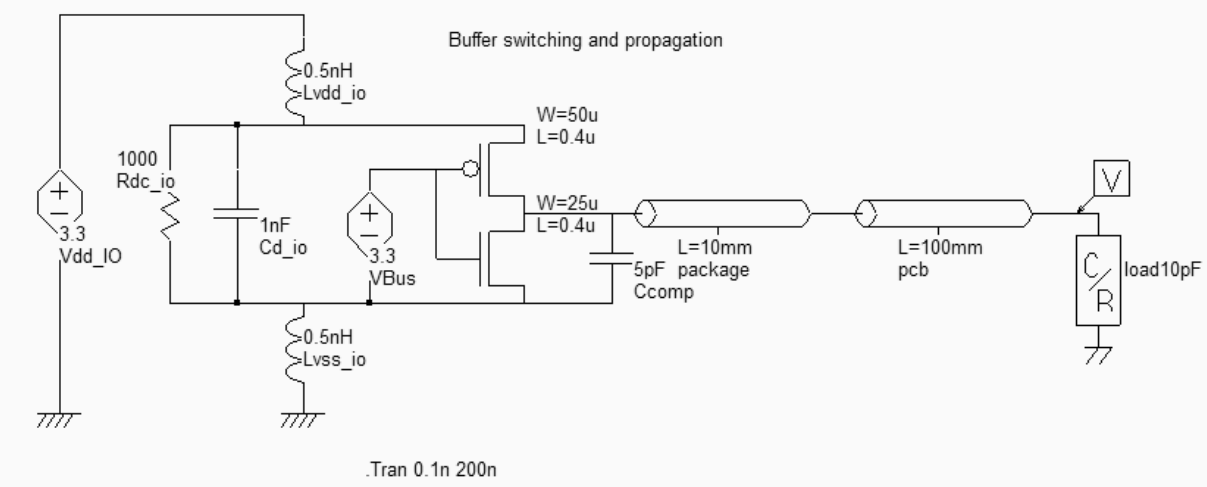



*Figure 8-2: driver loading a 100mm line and a 10pF termination (io_pcb.SCH)*

Note: the evaluation of the R,L,C parameters for the RLC lines (Package 10mm, Pcb 100mm) is performed using Delorme formulations for C and L, and a simple evaluation of the DC resistance. The model is based on a C/2-R-L-C/2 circuit as shown in figure 8-3. These formulations are accessible through the menu "EMC →Interconnect Parameters" of IC-Emc.

For example, the R,L,C parameters computed for the package are based on geometrical configurations typical for the BGA package (100µm width, 150µm separation to ground plate, 35µm thickness).

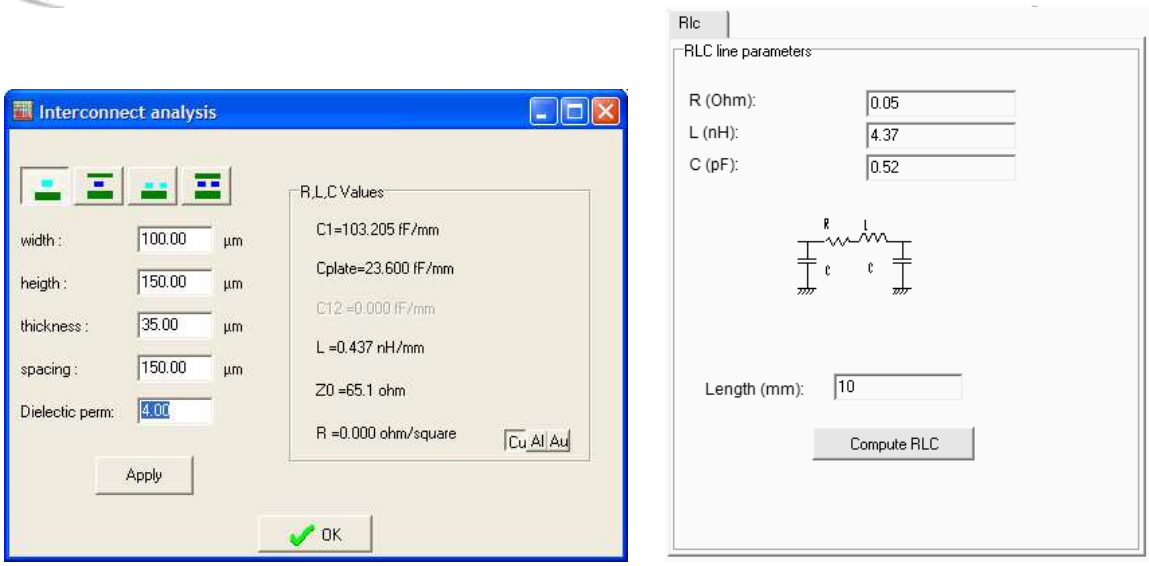



*Figure 8-4* : 10mm line R,L,C evaluation in IC-Emc

The simulation of the I/O switching at a rate of 66MHz (15ns period) is given in figure 8-5. We see the far end of the line close to the termination load (10pF).

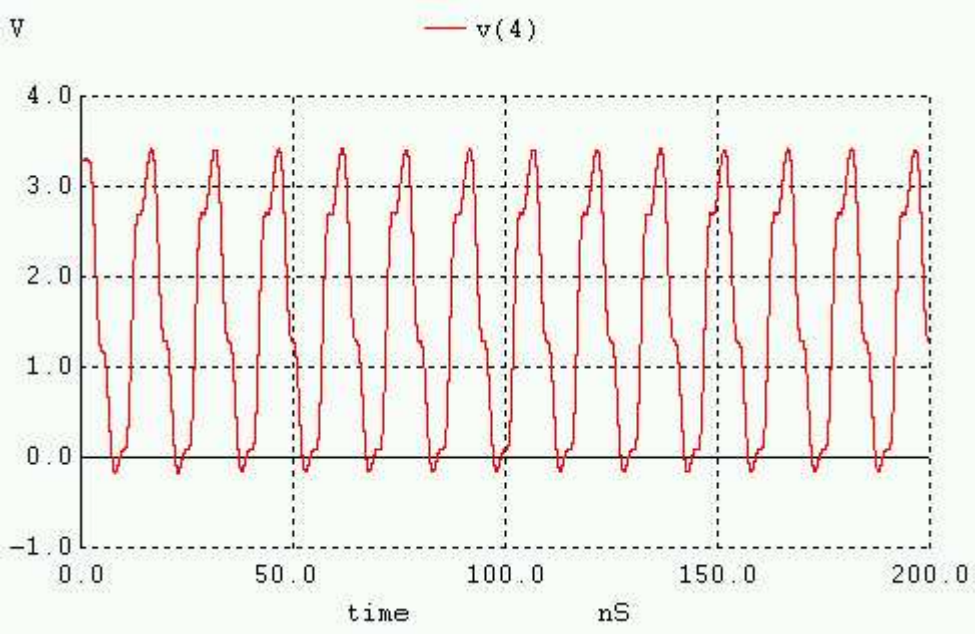



*Figure 8-6*: Waveform at the pad output (left) and the load (right)

## 8.2 Simultaneous switching noise

The study of the simultaneous switching with 8 output buffers is performed in this paragraph. We use the "inverter" symbol which includes the n-channel and p-channel MOS devices (Figure 8-7).

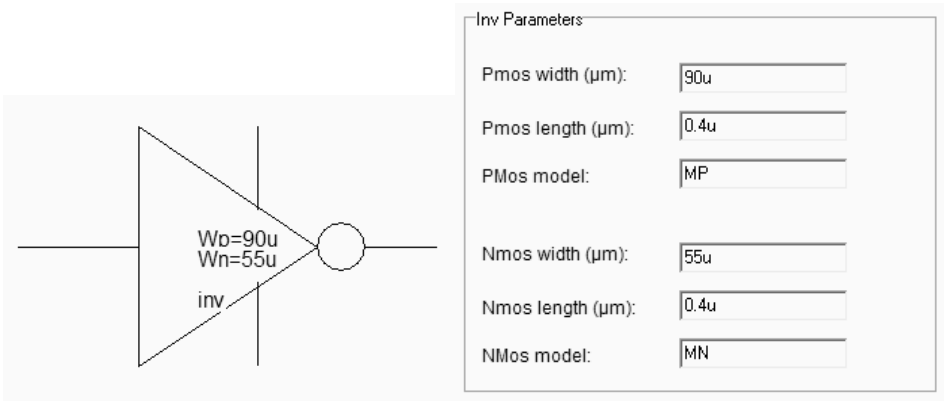



*Figure 8-8*: The Inverter includes the PMOS and NMOS device characteristics

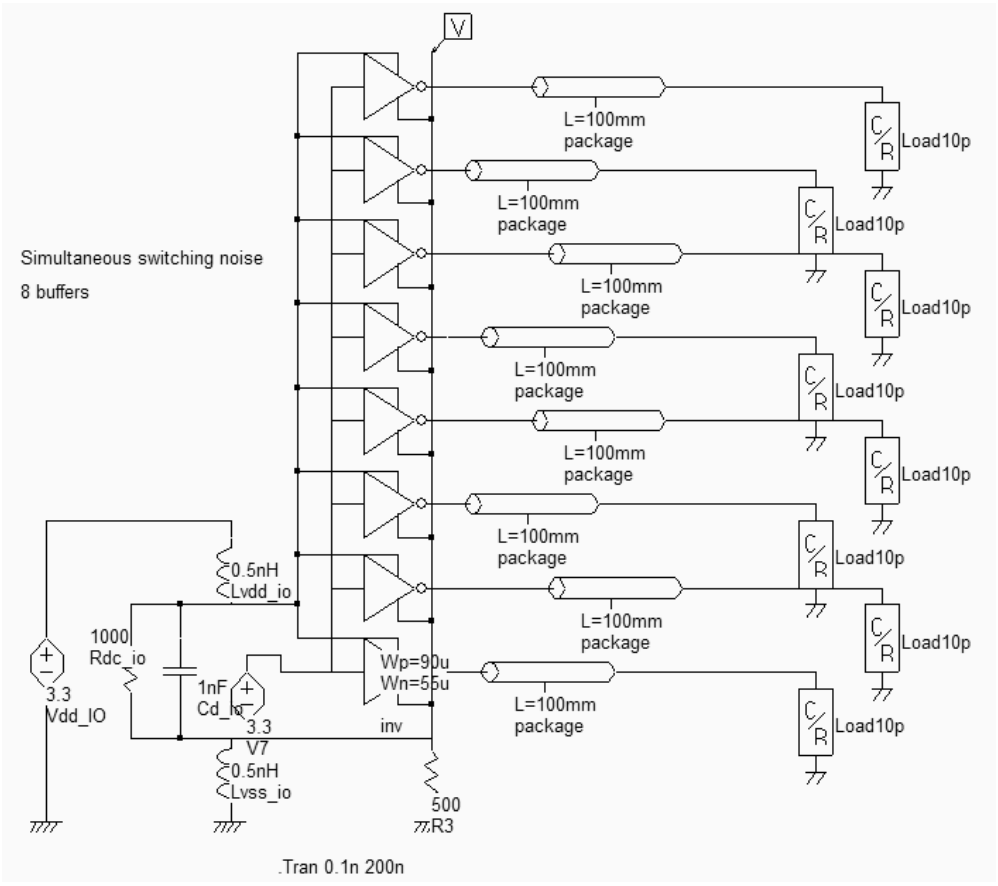



*Figure 8-9*: Simultaneous switching of 8 output ports with 100mm line and 10pF load (io_ssn.sch)

An example of synchronous switching of 8 output ports is proposed in figure 8-10. The 8 inverters are driven by the same clock. The supply are common, with a 0.5nH equivalent inductance to ground. The resulting switching noise is very high, as seen in the simulation of figure 8-11. Notice that each buffer is driving a 100mm line and a 10pF load.

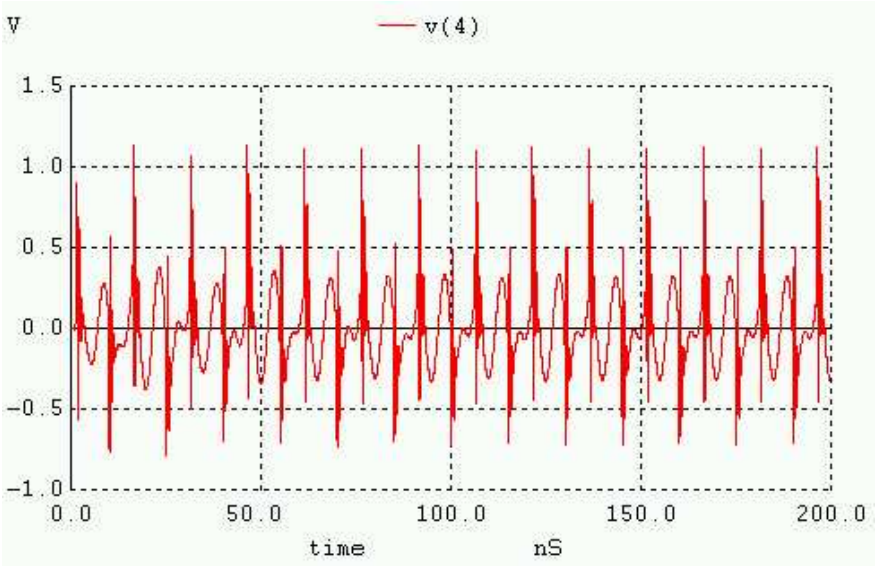



*Figure 8-12 :* Ground bounce on the IC near 1V (io_ssn.sch)

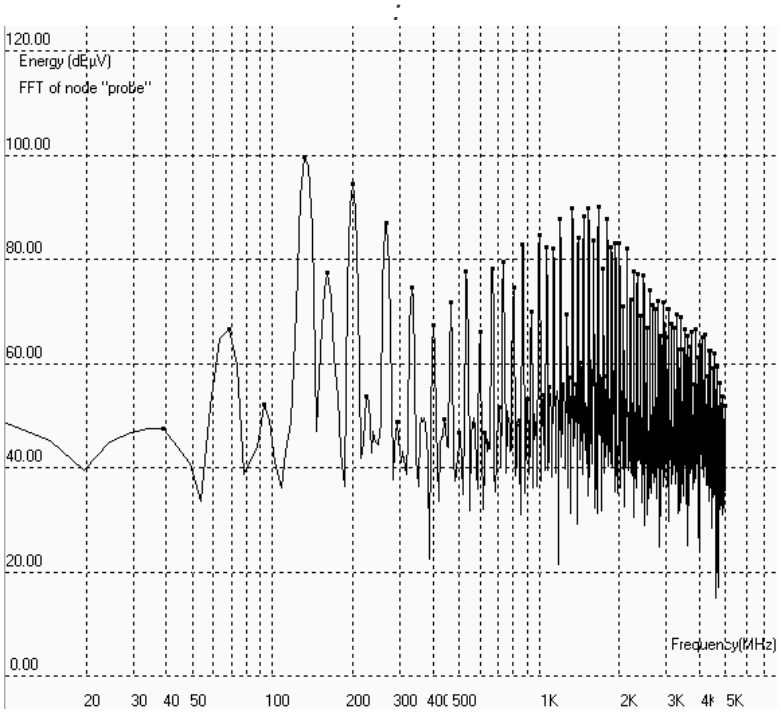



*Figure 8-13* Ground-bounce spectrum on the VSS_Io due to 8 buffer SSN (io_ssn.sch)

The ground-bounce spectrum is shown in figure 8-14. It can be seen that the 66MHz clock generates a complex series of harmonics contents. The main peak is observed at 133MHz.

# 9 Near-field scanning

Near field scanning has been widely used to exhibit “hot spots” at the surface of integrated circuits and to guide IC designers for reducing the parasitic emission [11]. The link between electrical macro-models such as ICEM and the near-field scanned information is investigated in this paragraph.

The CESAME test chip is dedicated to the characterization of conducted and radiated emissions from six identical logic cores, each having a specific design technique which aims to reduce parasitic emissions. The main goal of the test chip was to validate these design rules and to quantify the benefits in terms of reduced parasitic interference. The most interesting results have been presented in [12].

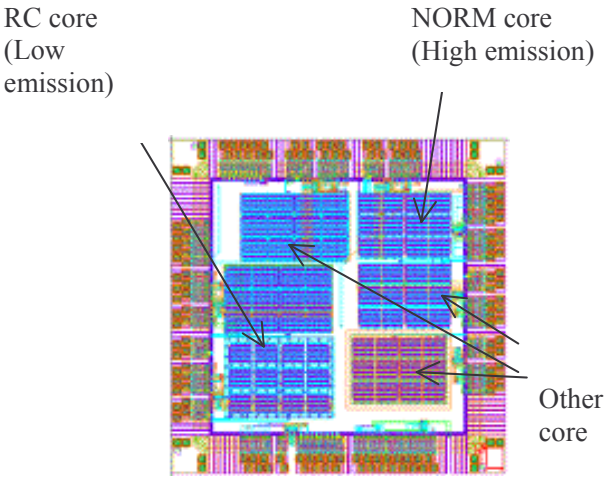



*Figure 9-1: The CESAME test chip*

The internal structure of CESAME is outlined in Fig. 9-2. Six logic core blocks are implemented in the same die. All these blocks have an identical structure based on latches, a clock tree and standard gate which reflect a standard core activity. Among these cores, two structures are worth of interest in our study: the normal core called “NORM” which is supposed to be noisy, and the “RC” core with includes a series resistor on the supply tracks and a local on-chip decoupling to feature low parasitic emission.

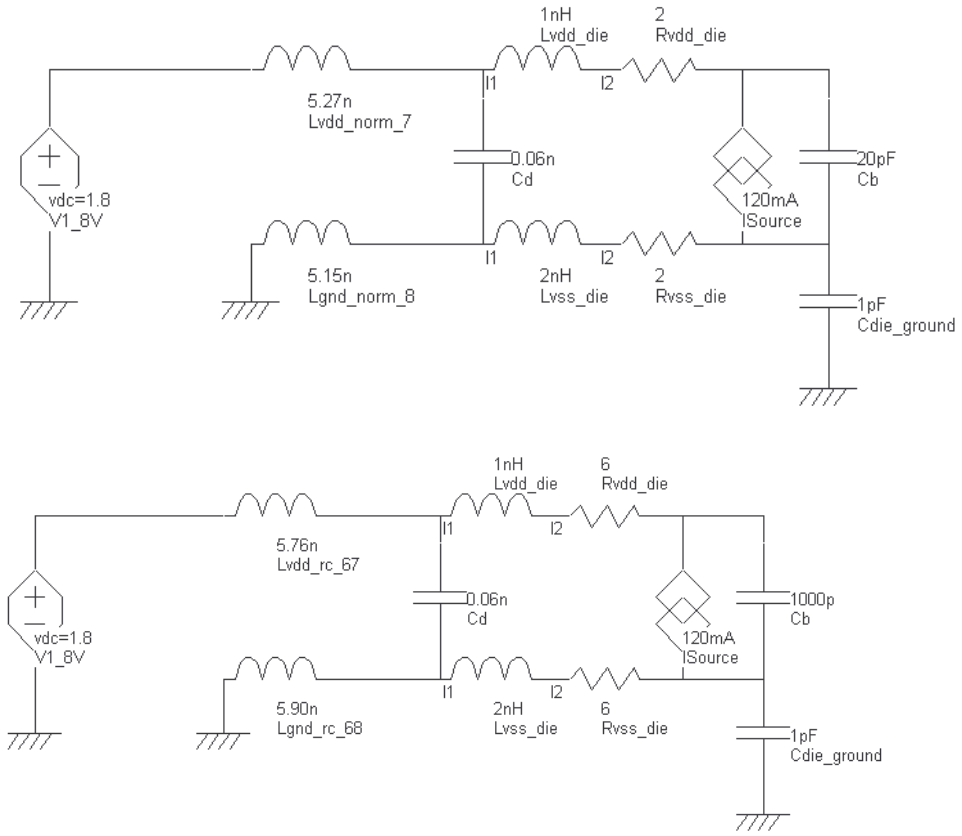



*Figure 9-3: schematic diagram of the NORM Core (upper figure) and RC core (lower figure)*

An electrical model has been setup and may well predict the emission of the two different cores. The schematic diagram of the CESAME cores are shown in figure 9-4. As can be seen on the right part, the current sources *ISOurce* are identical for NORM and RC core. The main difference concerns the serial resistance (*Rdd_die, Rvss-die*) and the local decoupling capacitance *Cb*. The access inductance of the package is almost the same for RC and NORM cores. Good correlations between measured and simulated spectrum according to IEC 61967 standard have been demonstrated. From these bases, our goal is to extrapolate the near-field magnetic field.

The measurement of near-magnetic field has been performed by our project partner at IZM [13]. The *Hx* and *Hy* contributions to the magnetic field have been measured separately using a magnetic field probe consisting of a loop mounted on a scan table, as illustrated in figure 9-5.

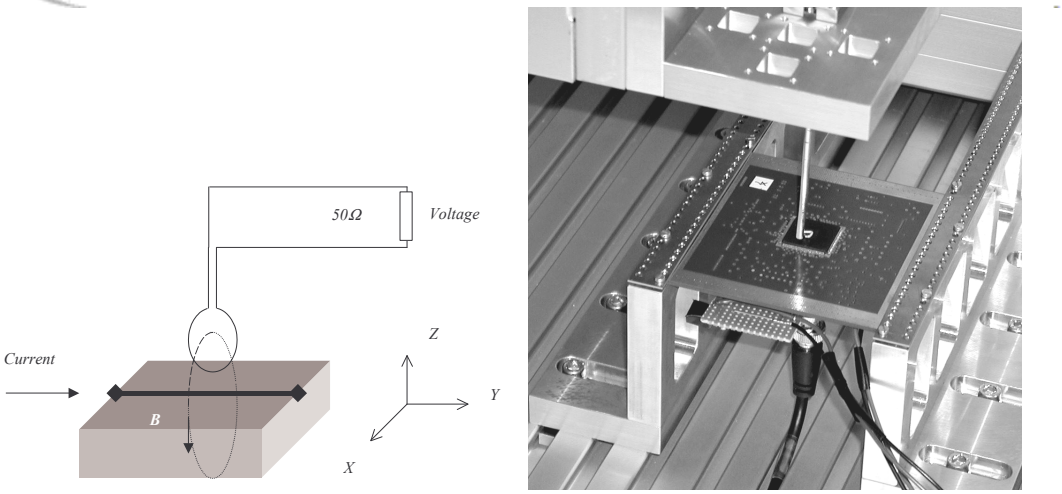



*Figure 9-6 : Principles for near field scan of the magnetic field*

The general flow used to achieve a comparison between near-field measurement and simulated magnetic field emission is proposed in figure 9-7. The CESAME test pinout chip has been described in an IBIS format [[14]], with details on the package parasitic R,L,C. In parallel, the electrical model of the core and supply network is given by the ICEM model. The analog simulation is performed by a Windows SPICE, while the Fourier Transform, current dipole magnetic prediction and user's interface is embedded in a specific tool IC-EMC developed for this study.

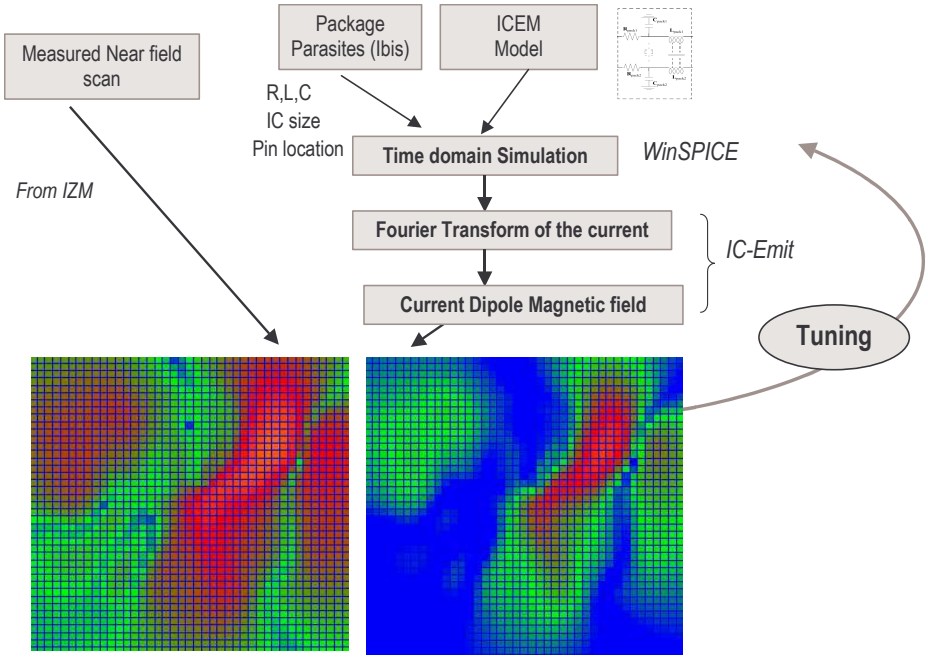



*Figure 9-8 : Proposed methodology to compare measured and simulated near field*

The key idea of the magnetic field simulation is to consider the CESAME circuit as a set of current dipoles. Each dipole is associated to each package lead inductance. This means that in first approximation, each core of the CESAME test chip may be represented by two dipoles, one for the VDD current, one for the VSS current. The current flowing inside the IC itself is neglected. Only remains the lead current.

```
|
[Package model] qfp
|pack_width=20e-3
|pack_height=20e-3
|ic_width= 2.7e-3
|ic_height= 2.5e-3
|pack_pitch=0.5e-3
|ic_altitude = 0.8e-3
```

*Figure 9-9 : Physical parameters added to the IBIS model of CESAME to account for the package and die size*

The package and die size information text are added in the [package model] section, in the IBIS file. The comment is mandatory to avoid parsing errors with conventional IBIS readers. However, IC-EMC can locate '|pack_' and '|ic_' keywords and get the relevant information.

The magnetic field generated by of each elementary current dipole is calculated from the well know formation reported in figure 9-10, where *l* is the length of the current dipole, *I0* is the current amplitude in the dipole (A), and $\omega=2\pi.f$ (rad/s).

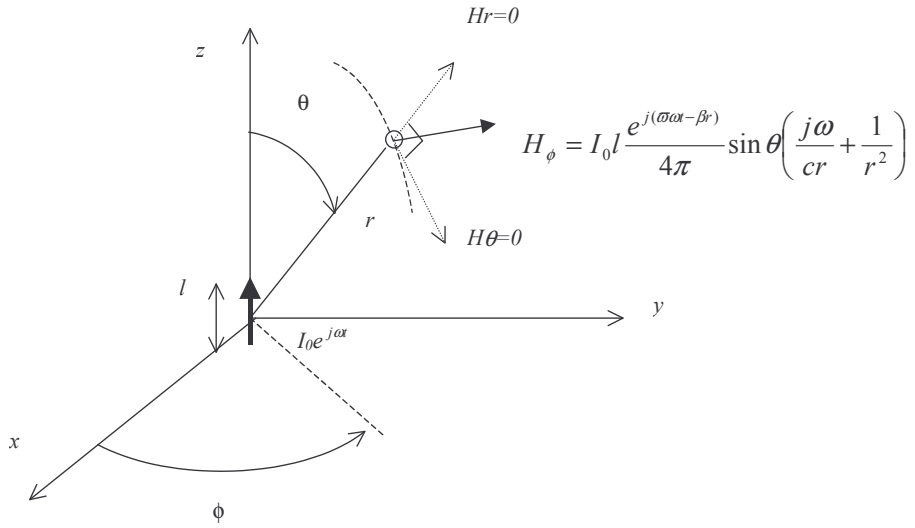



*Figure 9-11 : The magnetic field from an elementary dipole*

The formulation of the magnetic field is only valid if the dipole length is much shorter that the distance r to the observation point. As the scan was performed at the altitude of 2mm, the current dipole length is set to 500µm. Each lead of the package is split into elementary dipoles as shown in figure 9-12. The software code has first been prototyped and validated under Scilab [15], and compared with a full 3D field solver [16].

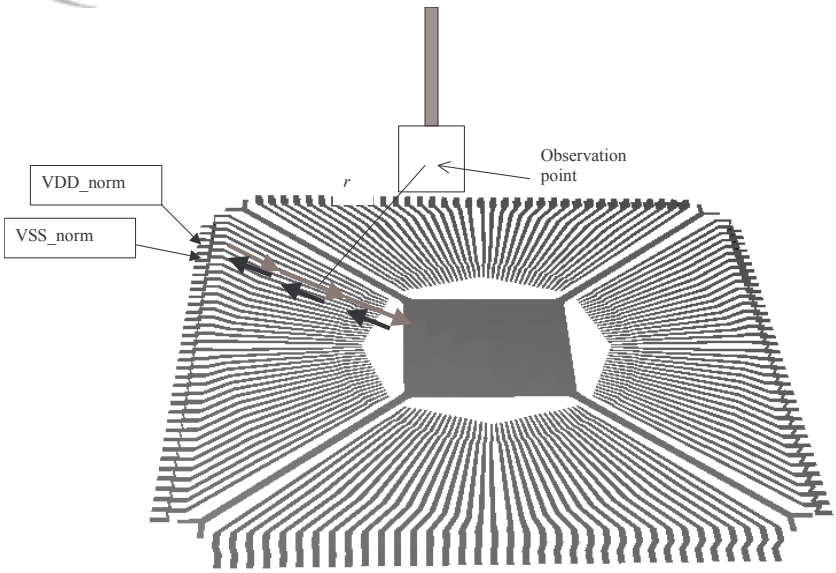



*Figure 9-13 : Each lead is considered as a series of elementary dipoles*

The magnetic current at the observation point is the sum (in complex domain) of all elementary currents flowing in the VDD and VSS leads of the package. As VDD and VSS wires are routed very close, the magnetic field tends to cancel at a certain distance above the surface of the integrated circuit. An adaptation of the formulation to our practical case is required as the current is not a pure sinusoidal wave as for the theory, but a pulse (Figure 9-14), which gives a reasonable approximation of the real on-chip current.

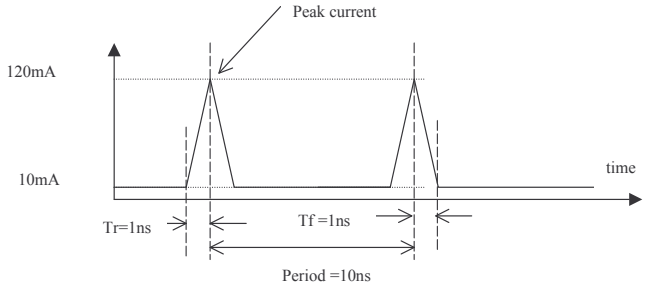
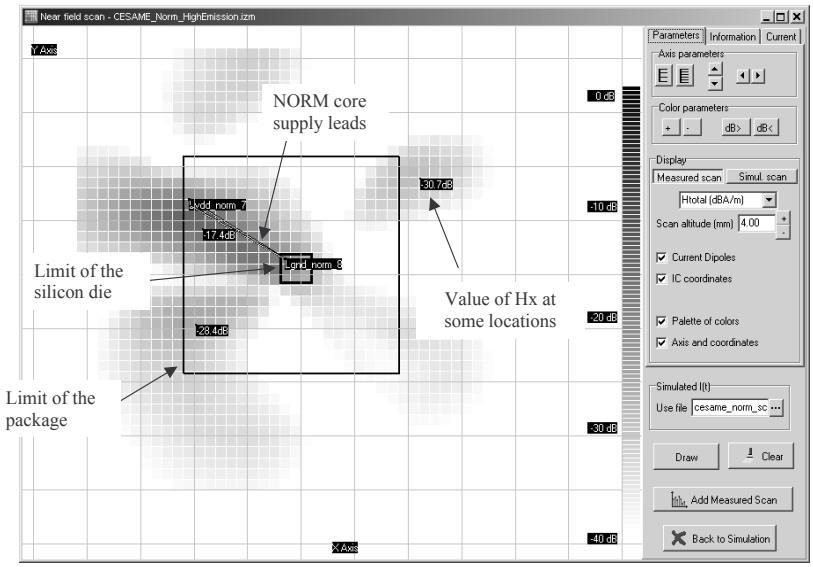



*Figure 9-15 : The approximated current pulse used in the ICEM model of the NORM and RC Core*

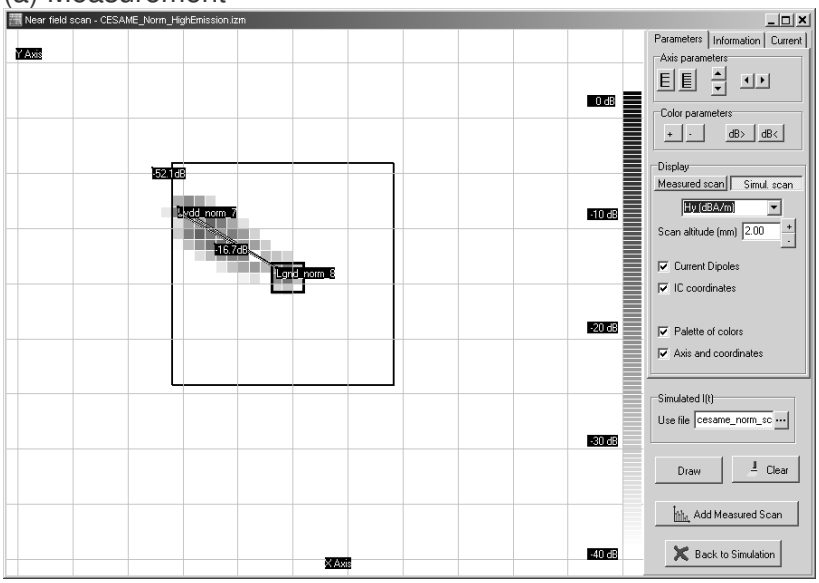
## 9.1 SPICE Simulation Results

The WinSPICE simulation is performed in time domain in order to monitor all currents flowing in all inductances. For each current *I(t),* a Fast Fourier Transform is automatically performed to extract the current amplitude *I0* to be injected in the dipole equation, at a given pulse ω. In the case of the NORM core, the IC-Emc user interface shown in figure 9-16 displays the position of the die, the package, and the position of the two main current dipoles. The SPICE simulation result is reported in the upper right corner of the window. It can be seen that VSS and VDD are not exactly equal, which has been confirmed by on-chip sampling [17]. At 100MHz, the current amplitudes are 4.6 mA for VDD and 22 mA for VSS.

The measurement of the magnetic field has been performed on the CESAME test chip by A. Tankielun. The *Hx* contribution of the magnetic field measured at 2mm above the ground plane is shown in figure 9-17 -a. The peak magnetic field is –17dB near the main dipole. Three other regions exhibit magnetic field around 20dB lower that the main region.




(a) Measurement




(b) Simulation

*Figure 9-18 : The measured and simulated magnetic field Hx for CESAME NORM core*

The distance between the measurement plane and the package lead-frame is estimated around 1mm. Consequently , the current dipole length has been set to 500um, according to the assumption that the current dipole length should be smaller than the observation distance.

The simulated magnetic field at an altitude of 2mm above the board surface is reported in figure 9-19 -b. It can be seen that the energy is only distributed among the package lead, as

expected. The peak magnetic amplitude is –17dB. Decreasing the elementary dipole length to 100µm do not change significantly the simulation and the peak magnetic field.

## 9.2 Multiple Return path model

It has been proven that the return path of the ground current is not only the VSS pin of the core but also the other VSS connections of other cores, due to a common substrate. The coupling via the substrate is considered in the model shown in figure 9-20 as a resistance, which has be characterized in DC to a value of 30 Ohm. The three inductance path correspond to the three core sharing the silicon bulk, weakly coupled to ground.

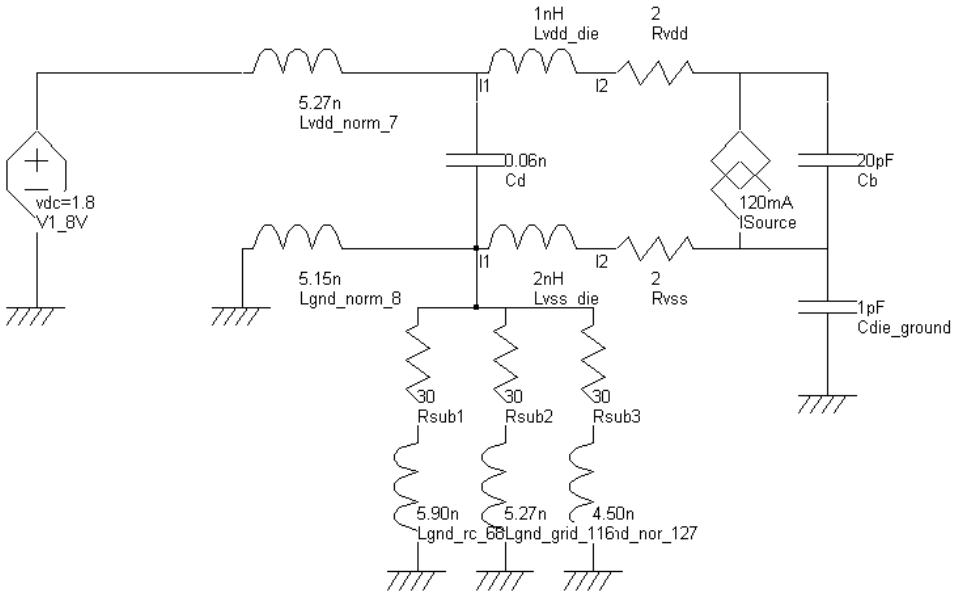



*Figure 9-21 : The multiple return path for the current due ti the share substrate*

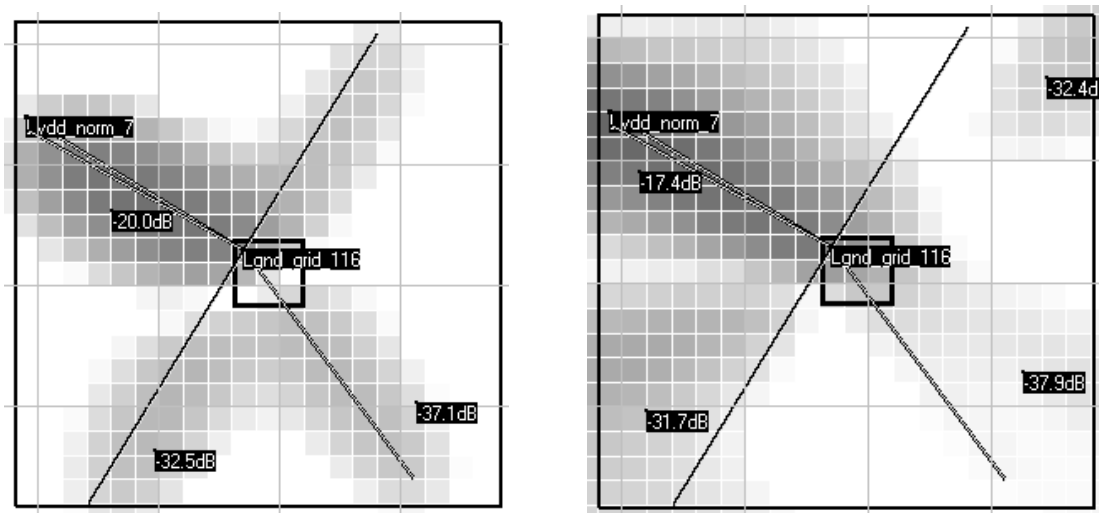



*Figure 9-22: The simulated (left) and measured (right) magnetic emission of the NORM core in CESAME test chip*

The simulation starts to behave closer to the measurements, as shown in figure 9-23. The

simulation is based on one VDD current dipole and four VSS current dipoles. The magnetic field appears above each lead, which is somehow what we measure on the surface of the IC (Figure 9-24-right). However, the energy is not exactly located at the position corresponding to the VSS leads.

# 10 Immunity Simulation

## 10.1 Introduction

This section is dedicated to immunity simulation, based on the reuse of ICEM models. Susceptibility to radio frequency interference is becoming a major concern for integrated circuits, with the multiplication of powerful parasitic sources such as mobile phones, high speed networks and wireless systems (Fig. 10-1). The trend for micro-miniaturization has two main consequences on integrated circuits (ICs) immunity. First, the constant supply voltage decrease reduces the noise margin of electrical signals and thus increases the IC susceptibility to RFI. Secondly,

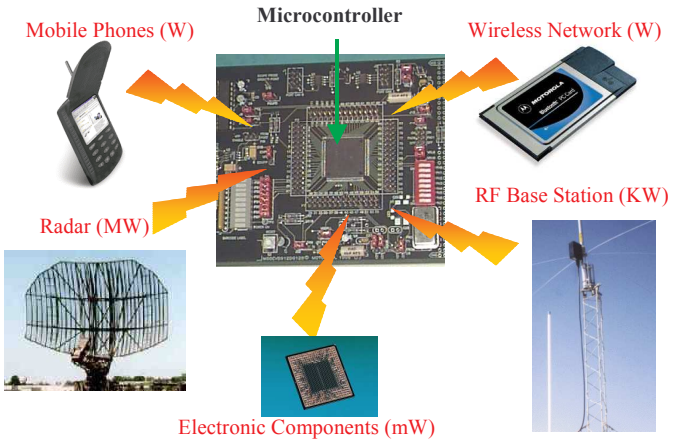



*Figure 10-2: Parasitic radio-frequency sources which may aggress integrated circuits.*

## 10.2 Direct Power Injection

A set of susceptibility measurement methods have recently been standardized by IEC [18]. A discussion about these methods may be found in [19].The direct power injection (DPI) method allows to measure the IC susceptibility level with capacitance coupling directly on the integrated circuit (Fig. 10-3). The test setup uses a specific printed circuit board on which the device under test is placed. The injection is performed through a coupling capacitance *Cdpi* operating within the frequency band 10 kHz to 1GHz.

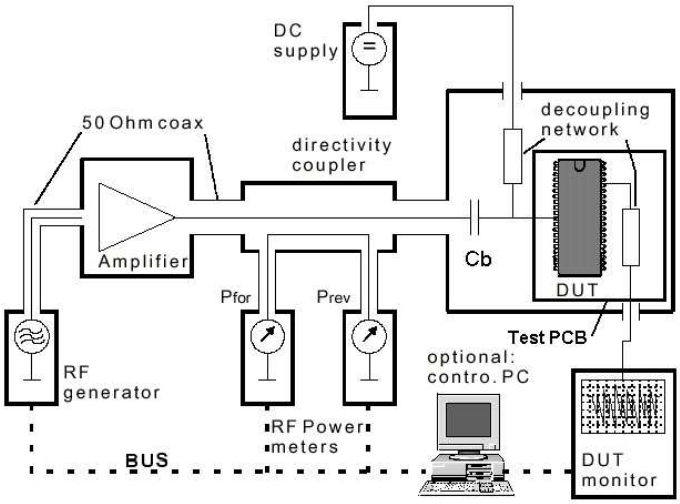



*Figure 10-4 : Set-up for immunity testing using DPI method.*

## 10.3 Comparison between measured and simulated susceptibility

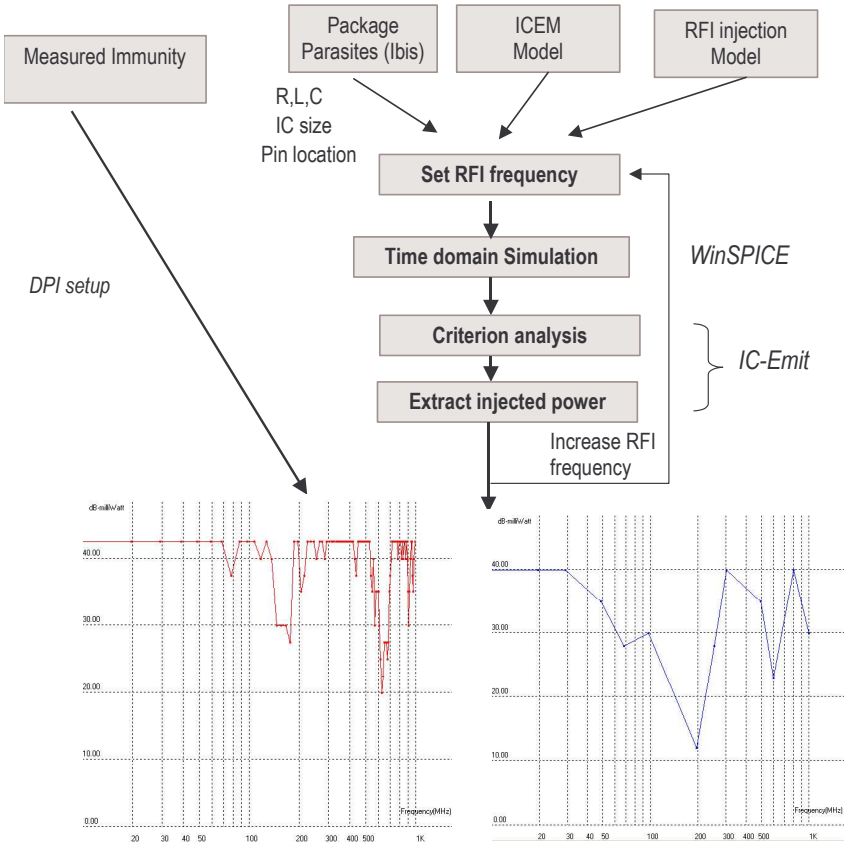



*Figure 10-5 : Proposed methodology to compare measured and simulated immunity of Ics in Direct Power Injection mode*

The general flow used to achieve a comparison between bulk current injection measurement

and simulated susceptibility is proposed in figure 10-6. The measurement of BCI immunity is performed using the standardized test bench. The result is the forward power in dB-milliwatt (dBm) versus frequency. For the simulation, we rely on package information given by IBIS, the core model given by ICEM, and the injection model including the RFI generator, the cable and the coupling capacitance.

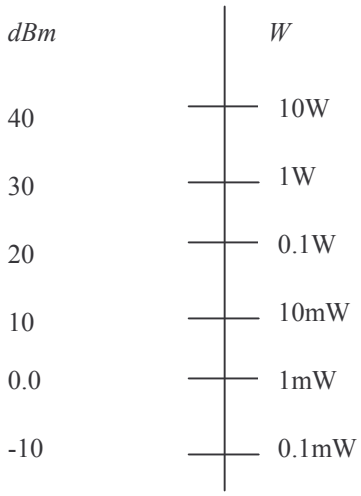



*Figure 10-7: Correspondence between dBm and Watts*

## 10.4 Radio-Frequency Source

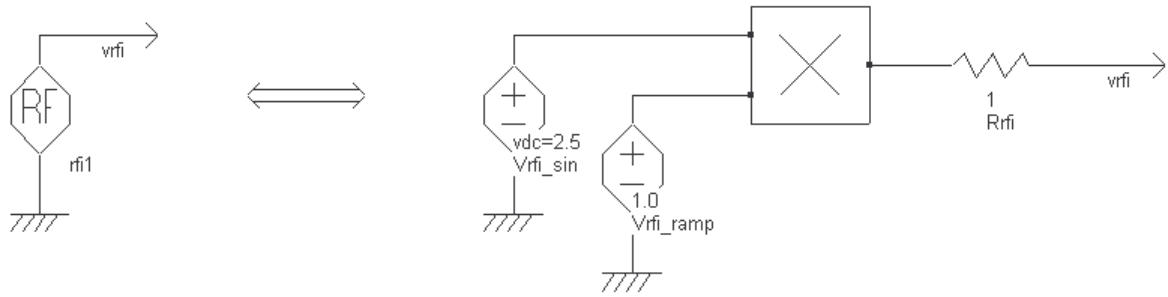



*Figure 10-8 : The RFI source includes two multiplied voltage sources and a 1 ohm resistance (ICIM_rfi.SCH)*

The RF source is a sinusoidal wave with programmable slope. There exist no generic voltage source in WinSPICE to generate such a source. Therefore, the source is built from two voltage sources, VRFI_sin and VRF_ramp, that serve as inputs for a “B“ element, which performs V(RFI)= VRFI_sin* VRF_ramp. Also notice the $R_{RFI}$ element of 1 ohm that is required for the monitoring of the current and voltage, in order to compute the power delivered by the voltage source.

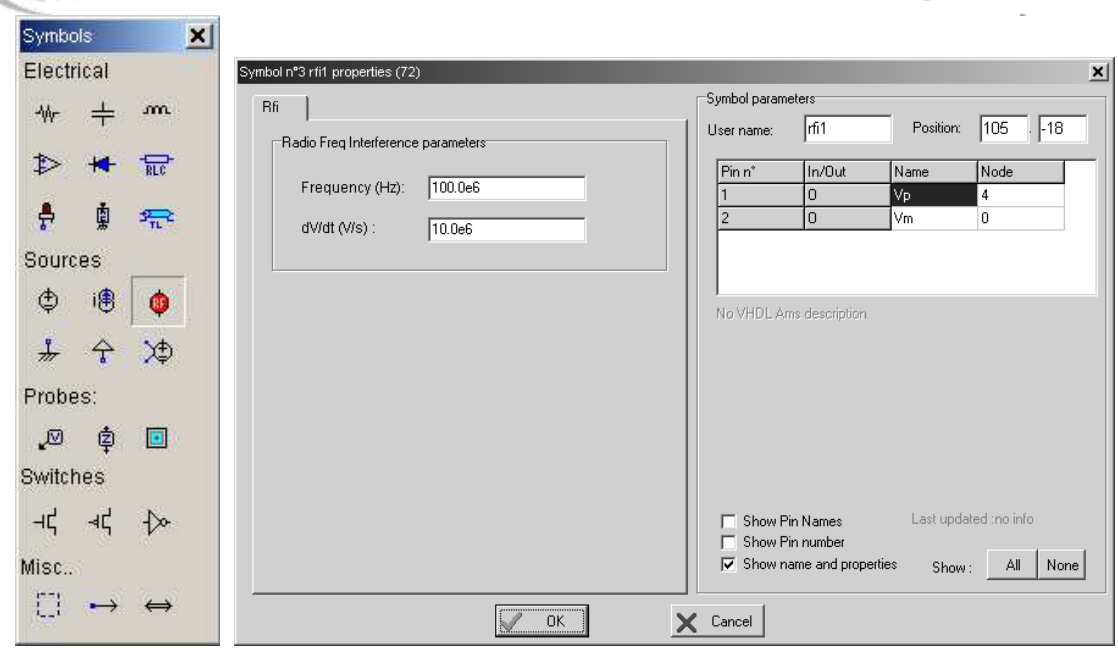



*Figure 10-9: Injection source parameters*

The injection source parameters are listed in figure 10-10. The frequency is the first important parameter, followed by the ramp in V/s. In our case, the ramp is equivalent to 10V/µs.

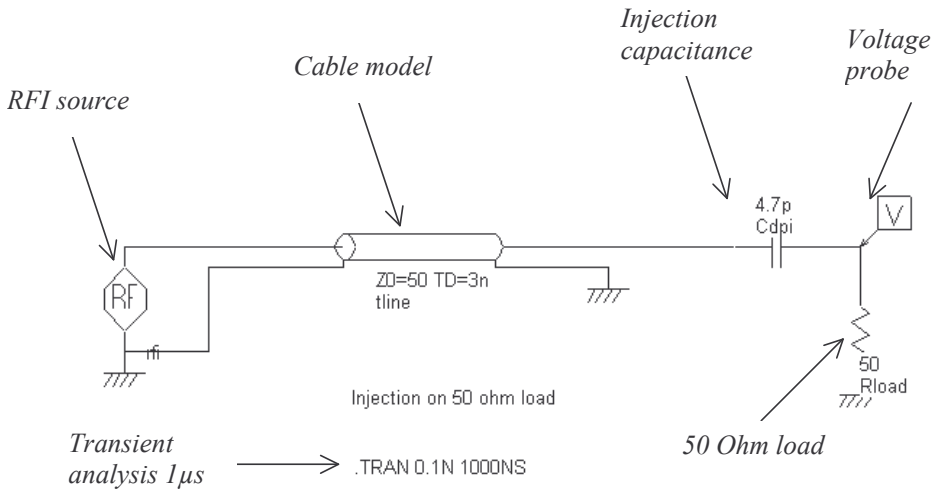



*Figure 10-11: Injection model (ICIM_rfi_50Ohm.SCH)*

An example of injection model is given in figure 10-12. The cable uses the transmission line model, the injection element is a 4.7pF capacitance *Cdpi*, and we test the injection on a 50Ohm load modeled as a resistance *Rload*. Launch the WinSpice simulation on the SPICE file “icim_rfi_50Ohm.CIR”. The result shown in figure 10-13 appears. The green chronogram corresponds to the primary voltage source Vrfi. The red curve corresponds to the voltage delivered to the 50ohm load.

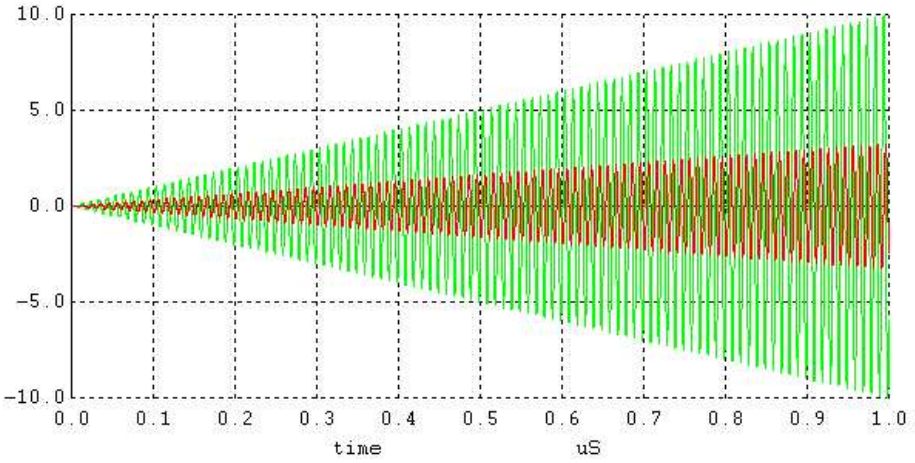



*Figure 10-14: Injection simulation on a 50Ohm load (ICIM_rfi_50Ohm.SCH)*

## 10.5 Injection to an integrated circuit

An example of susceptibility prediction concerning a micro-controller is given in figure xxx. The model includes the RF source, the cable, the injection capacitance that perturbs one inactive buffer. The buffer supply are shared with the core supply. The RF power goes to the core and modifies the internal voltage.

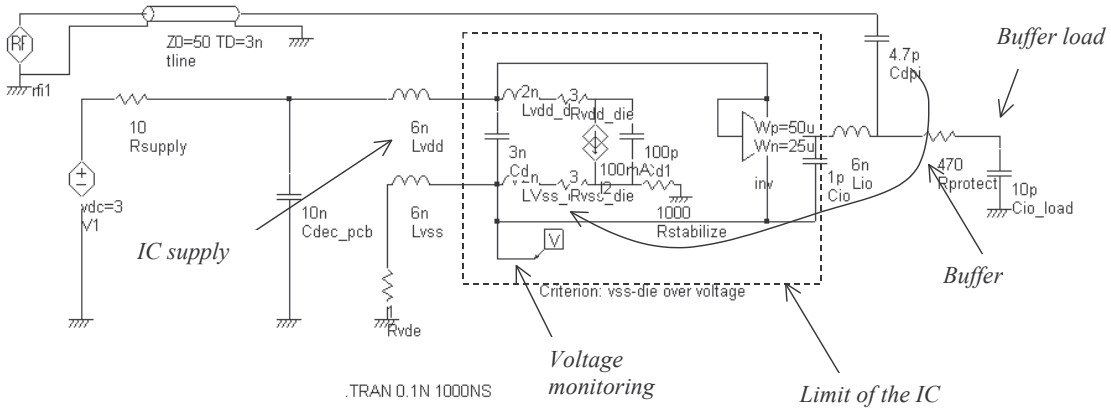



*Figure 10-15 : Example of DPI injection on an IC (ICIM_rfi_ic.SCH)*

The susceptibility criterion corresponds to a fluctuation of VSS_die over 30% of VDD (3V here). Click the “immunity icon”, and click “time” to observe the RFI voltage. At 100MHz, the VSS_die voltage shown in figure 10-16 do not reach the susceptibility limit 0.75V.

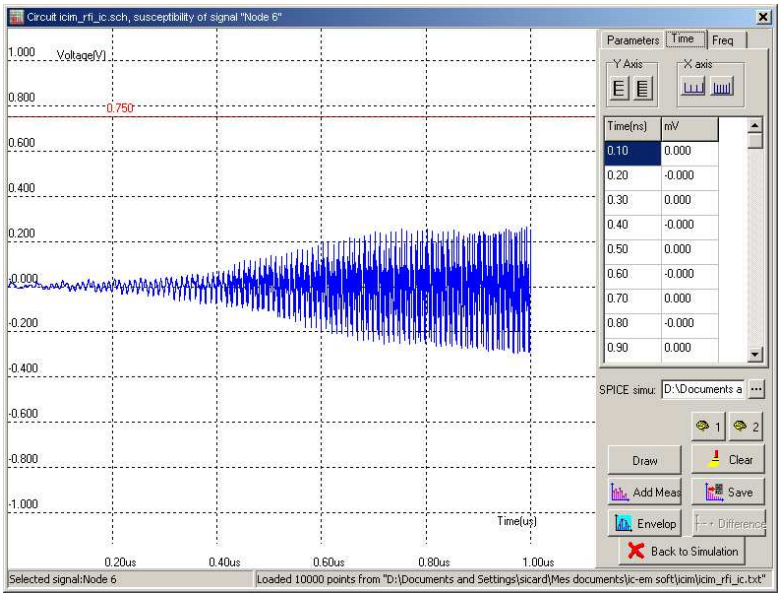



*Figure 10-17 : DPI injection on an IC at 100MHz (ICIM_rfi_ic.SCH)*

The control of the SPICE generation is shown in figure 10-18. First, the RFI frequency is changed, then, the user creates an update version of the CIR file. WinSpice produces the corresponding simulation. Click „Get Power“ to extract the source power at which the voltage limit has been reahed at the observation point.

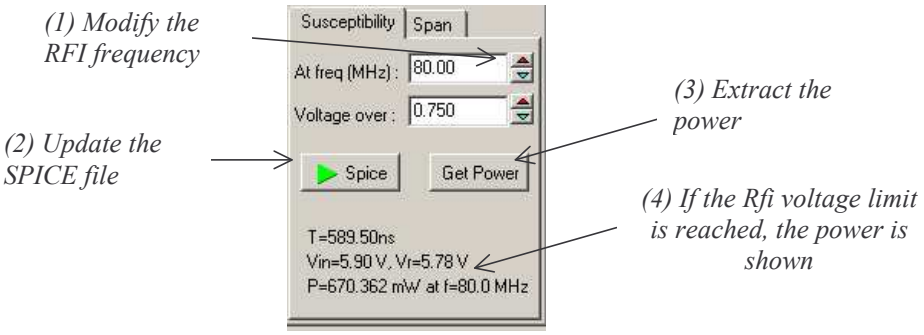



*Figure 10-19: Control of the RFI frequency and SPICE file generation and dBm extraction (ICIM_rfi_ic.SCH)*

For a 80MHz injection, the threshold limit is reached at t=589ns, where the voltage source delivers 670mW, equal to 28.3 dBm (Figure 10-20).

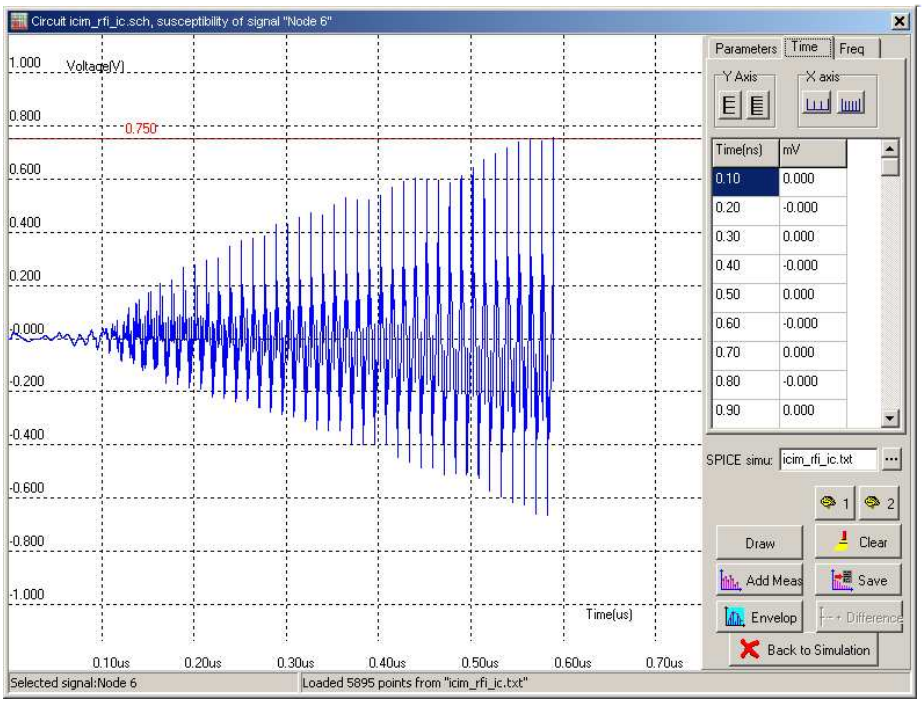



*Figure 10-21 : DPI injection on an IC at 80MHz (ICIM_rfi_ic.SCH)*

## 10.6 Future work

Thanks to iterative SPICE simulations, the correlation between measured and simulated immunity should be made available. Measured immunity results (Freq, dBm format) may be downloaded using the button “Add Meas”.

# 11 Conclusion

This report has described the implementation of ICEM model in a dedicated environment IC-EMC, and the comparison between measurements and simulations for several test chips.
The basic elements of the ICEM model have been used for modeling. A good agreement between measurements and simulations has been found with this simple approach, without the needs for fitting. The model parameters may be further refined to achieve a more accurate matching.
The interface with IBIS provided in IC-EMC software has also been described. The IBIS and simulated buffer characteristics may be easily compared.
In another chapter, extremely high frequency models for discrete capacitor have been proposed, based on [s] parameter measurements.
We also compared simulated and measured near-field scan information related to CESAME test chip, and described the flow used to achieve this comparison. Finally, we presented the specific screen used to compare simulated and measured immunity.

# 12 Other Tools

## 12.1 Resonant Frequency

The "Resonant Frequency" tool included in the EMC menu computes the impedance of L, C at a given frequency. The LC resonance is also computed, with its associated characteristic impedance (Figure 12-1).

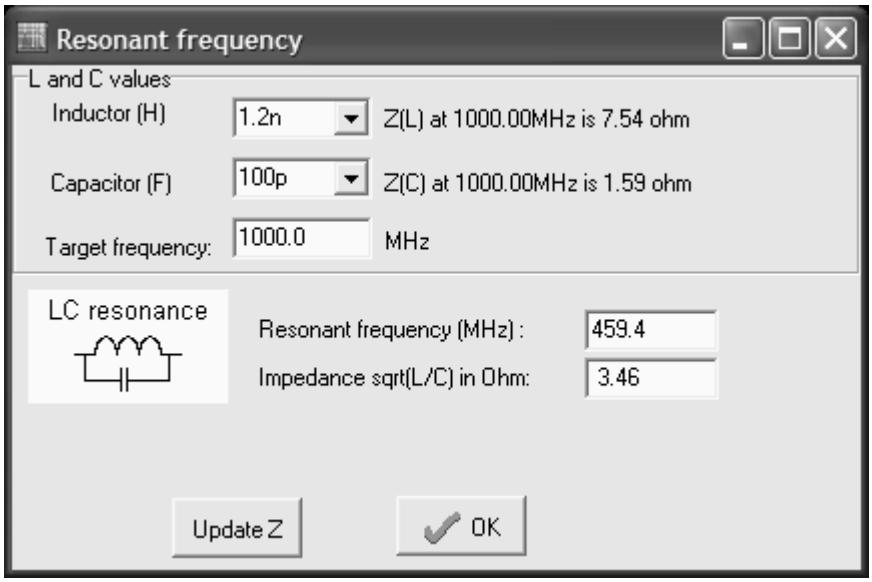



*Figure 12-2: Resonant frequency of given L and C, with associated impedance*

## 12.2 Interconnect Parameters

The "Interconnect parameters" tool included in the EMC menu computes the R,L,C parameters of an interconnect based on its physical dimensions. The Delorme formulations are used for this approximations [20].

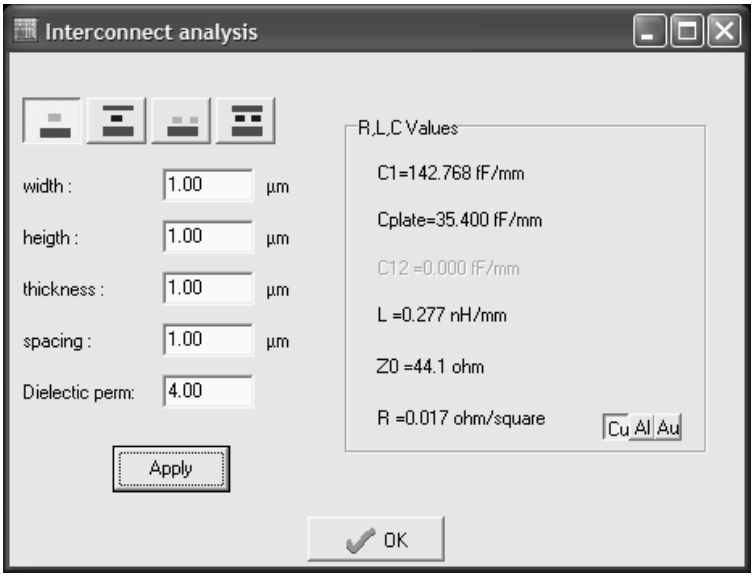



*Figure 12-3: Interconnect R,L,C model based on physical dimensions*

In the example of figure 12-4, a conductor above a ground plane has a plate capacitance of 35fF/mm, but a real capacitance around 143fF/mm. The inductance is close to 0.277nH/mm, and the characteristic impedance SQRT(L/C) is 44 ohm. The resistance is approximated from the cross-section and the conductor resistivity. Copper (Cu), Aluminum (Al) and gold (Au) may be selected.

## 12.3 Patch Antenna Resonant Frequency

The "patch" is a low gain, narrow-bandwidth antenna. Many types of vehicles concerned with aerodynamic considerations require such type of low-profile antennas. Typically, a patch consists of a thin conducting sheet about λ by ½ λ mounted on a substrate and isolated by a dielectric. The patch-to-ground-plane spacing is usually around λ/100. The patch length is designed based on the desired resonance with W=λ, while L is often constrained by availability of space in the electronic device. A practical choice of L is λ/2. A larger L would increase efficiency but higher order modes might distort the radiation patter.

The formulation for the resonant frequency of the patch antenna depends on its physical dimensions W and L, as follows:

$$f_{mn} = \frac{1}{2\sqrt{\mu\varepsilon}}\sqrt{\left(\frac{m}{L}\right)^2 + \left(\frac{n}{W}\right)^2}$$

where

fmn=frequency (Hz)
ε= permittivity = $\varepsilon_0\varepsilon_r$
$\varepsilon_0$= 8.85x10$^{-12}$ F/m
$\varepsilon_r$= 3.8 (SiO2)
μ= permeability= $\mu_0\mu_r$
$\mu_0$= 4πx10$^{-7}$ H/m
$\mu_r$= 1 (Air)
m=mode (integer 0,1,2..)

n=mode (integer 0,1,2..)
L=length of patch (m)
W=width of patch (m)

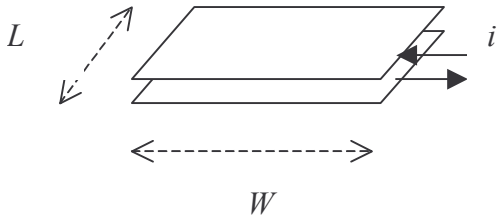



*Figure 12-5 : the patch antenna*

In susceptibility analysis, the IC may be considered as a resonant system in very high frequency (Figure 12-6). The screen “Patch Resonant Frequency” computes the resonant frequencies according to the above formulation.

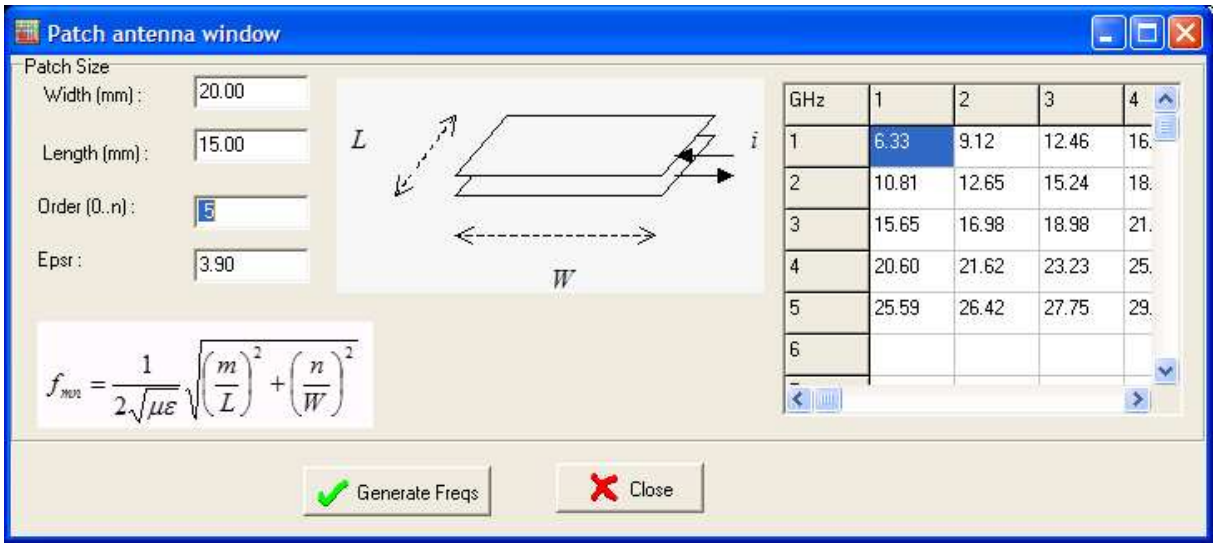



*Figure 12-7 : Computation of the patch antenna frequency*

# 13 Appendix

## 13.1 ADV Frequency File Format

The ADV format corresponds to raw data generated by the spectrum analyzer Advantest 3131 (1Mhz-3GHz). The text file format is: frequency (Hz), first column, followed by spectrum energy (dBµV).

"1010000","-7,6"
"1015000","-7,5"
"1020000","-7,0"
"1025000","-7,6"
"1030000","-7,1"
"1035000","-7,5"
"1040000","-7,0"
"1045000","-7,5"

## 13.2 TAB File Format

The TAB file format is generated by several equipments, and corresponds to a text document, organized with the frequency (Hz), first column, followed by spectrum energy (dBµV), followed by position.

| Fréquence (Hz) | Peak | Position |
|---|---|---|
| 10E6 | 2.11656 | 0 |
| 10.05E6 | -1.02154 | 0 |
| 10.1E6 | -4.87756 | 0 |

## 13.3 Z Format

Consists of the frequency, and the module of the impedance.

```
CAPA  Impedance
100pF A5 impedance vs frequency
Freq(Hz) Z(f)
45000000   25.96613733
57443750   15.90372125
69887500   10.70620745
82331250   7.724689023
94775000   5.852317536
```

## 13.4 S Format

Consists of the frequency, the real part of S11, and the imaginary part of S11. IC-Emc computes the module of the input impedance using the following correspondence. We note R `Real(s11)`, and X `Im(s11)`.

$$S11 = R + jX$$

$$Zin(real) = Z_0\left(\frac{1-R^2-X^2}{(1-R)^2+X^2}\right)$$

$$Zin(imag) = Z_0\left(j\frac{2X}{(1-R)^2+X^2}\right)$$

$$|Zin| = \sqrt{Zin(real)^2 + Zin(imag)^2}$$

```
PCB Board
Mesures S11(f)
Freq (Hz) Real(s11) Im(s11)
1000000 0.882568359     -0.468902588
1004326.68      0.881835938     -0.470703125
1008672.081     0.880554199     -0.472717285
1013036.282     0.87979126      -0.474334717
1017419.366     0.878875732     -0.476348877
1021821.414     0.877929688     -0.477966309
```

## 13.5 N7 Scan format

<Add info>

## 13.6 IZM Scan format

<Add info>

## 13.7 XML Scan format

<Add info>

## 13.8 Technology file example for configuring IC-Emc

```
ICEMIT 1.1 - technology file
NAME "CMOS 0.25um"
VERSION 11.10.2004
* Supply voltage
VDD = 2.5
* Typical gate delay in ns
TDelay = 0.100
* Typical current in mA
TCurrent = 0.3
```

```
* Gate activity from 0 to 100 (%)
GActivity = 10
* Parasitic capa in fF per gate
Cdecap = 7
* Parasitic capa in pF/mm2
Csurf = 15
* Package inductance in nH/pin
LDIL = 15
LQFP = 10
LPGA = 7
LBGA = 5
LUBA = 4
LCSP = 2
* Default MOS length and width
ML  = "0.25u"
MW  = "2.0u"
*
* End cmos025.tec
*
```

# 14 References

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[15] The SCILAB software may be download from http://scilabsoft.inria.fr/

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[17] Bertrand Vrignon, Sonia Bendhia, Enrique Lamoureux, and Etienne Sicard, « Characterization and modeling of parasitic emission in deep submicron CMOS”, IEEE transaction on EMC, to appear 2005

[18] International Electro-technical Commission "IEC 62132: Integrated Circuits, Measurements of Susceptibility", IEC standard. www.iec.ch; part 4 (group 47A) “Integrated circuits, immunity test to narrow-band disturbances by Bulk Current Injection (BCI), 10KHz-400MHz”

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